COAST GUARD ADDENDUM

DRAFT

AUSTRON 2000C RECEIVER

VOLUME 2OF 2

NOVEMBER 1977

DRAFT

COAST GUARD ADDENDUM TO AUSTRON 2000C RECEIVER TECHNICAL MANUAL VOLUME 2

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FIGURE

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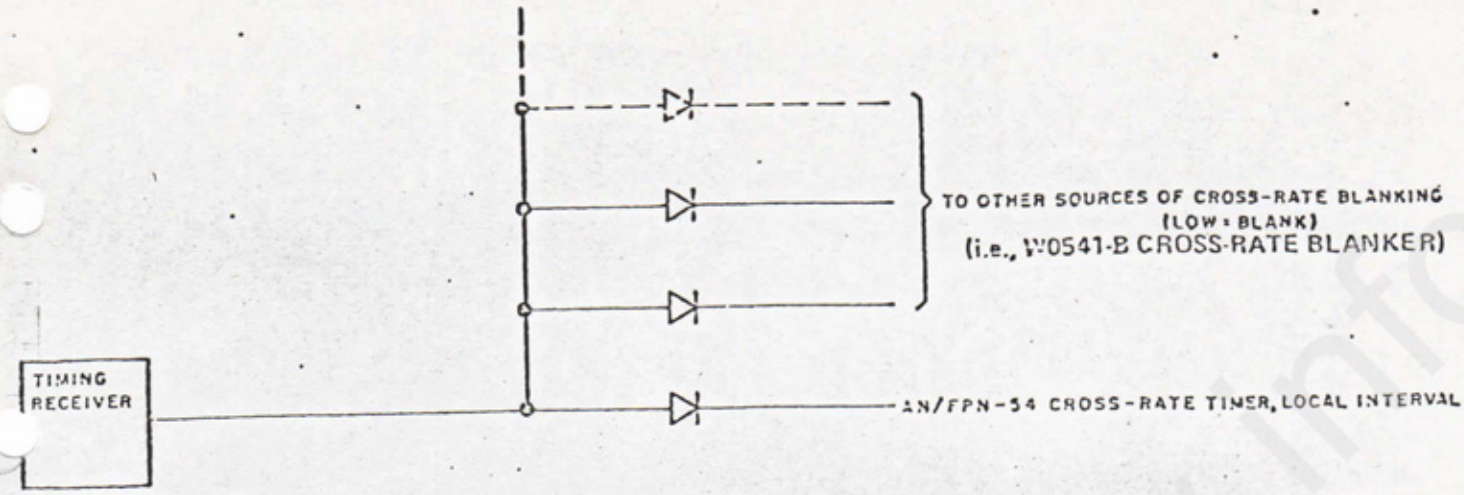


Figure 2-1

Method Of Multiple Cross-Rate Blanking

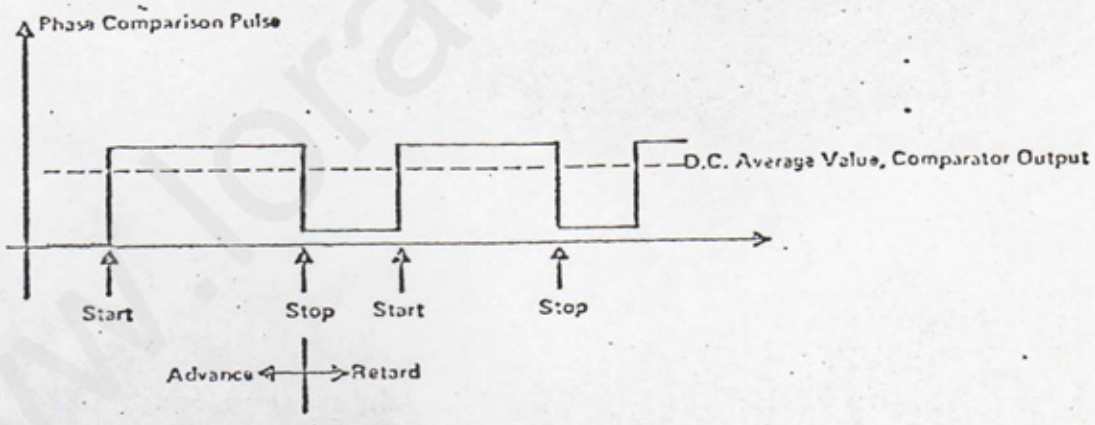


Figure 2-2

Definition Of Phase Comparator START—STOP Inputs

NOTE:
JUMPER CONNECTIONS
TERM. 3 TO 5 OR 3 TO 6

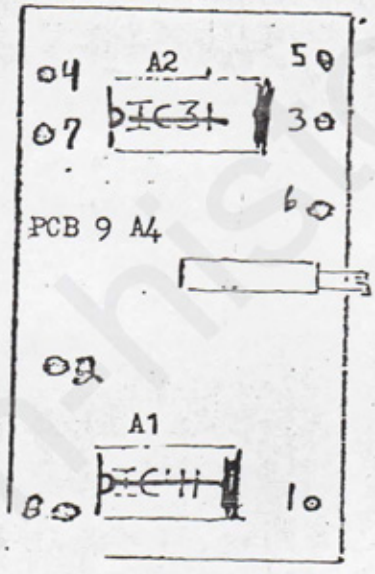


FIG. 2-3

ONE MICROSECOND PHASE COMPARATOR

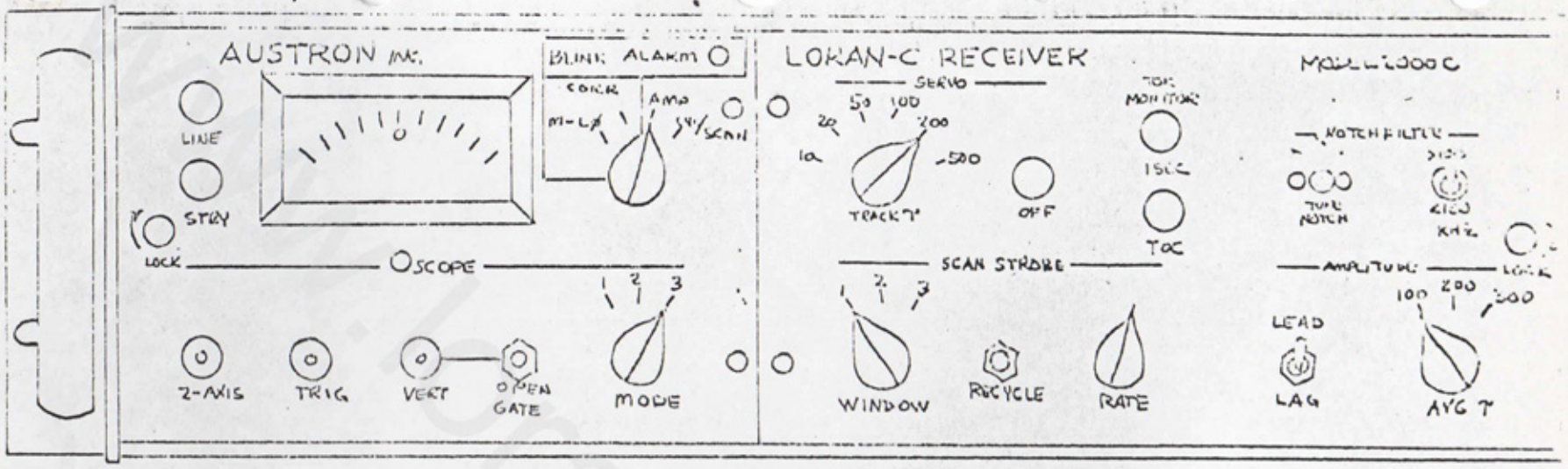
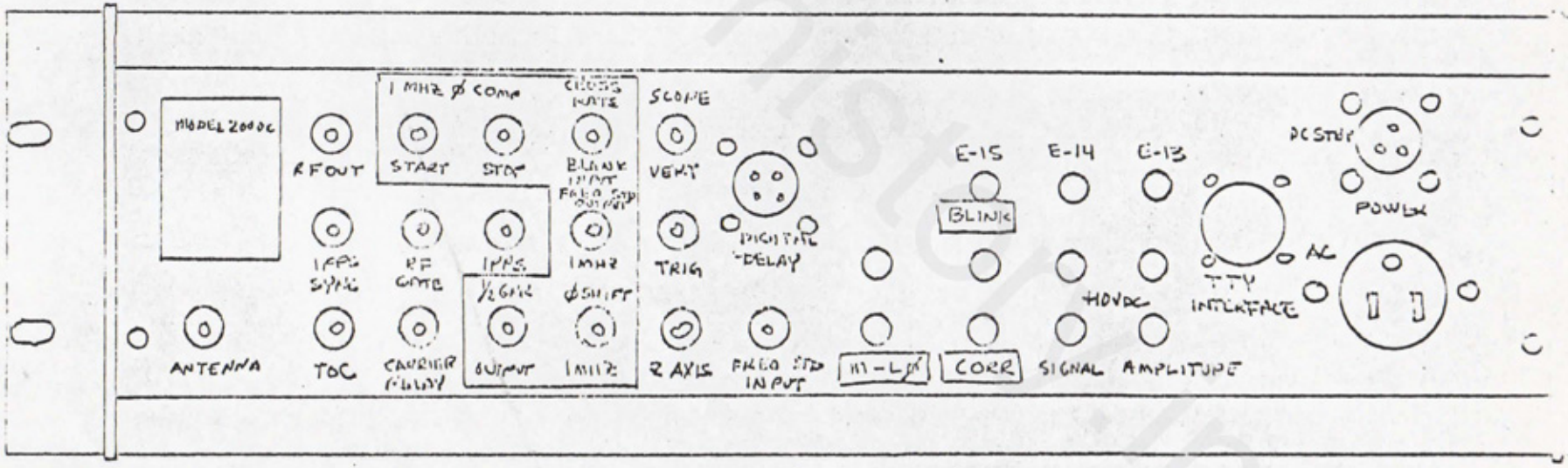


FIGURE 2-4



FRONT AND REAR PANEL CONTROLS AND INDICATORS

FIGURE 2-5

AUSTRON MODEL 2000CG LORAN-C RECEIVER

REAR PANEL MODIFICATIONS

	JACK	OLD LABEL	NEW LABEL	OLD TERMINATION	NEW TERMINATION
1.	J24	Phase Code	Start	J7-3C	J9-16F
2.	J23	1 kHz	Stop	J6-8C	J9-11F
3.	J22	10 kHz	X-Rate Blank Input	J6-9C	J8-12C
4.	J27	100 kHz	Freq. Std. Output 1 MHz	J6-10C	J9-3F
5.	J33	Ø Shifted 1 MHz	No change	J6-11C	No change
6.	J34	GRP	1/2 GRR	J8-4F	J8-7F
7.	E15 (New)	Blank	Blink Alarm	Blank	J12-5C
8.	E8	10 µs	M-LØ	J11-12F	No change
9.	E7	100 µs	CORR	J11-10F	No change
10.	E14 (New)	Blank	Signal (Green)	Blank	J3-15F
11.	E13 (New)	Blank	Amplitude (Green)	Blank	J4-15F

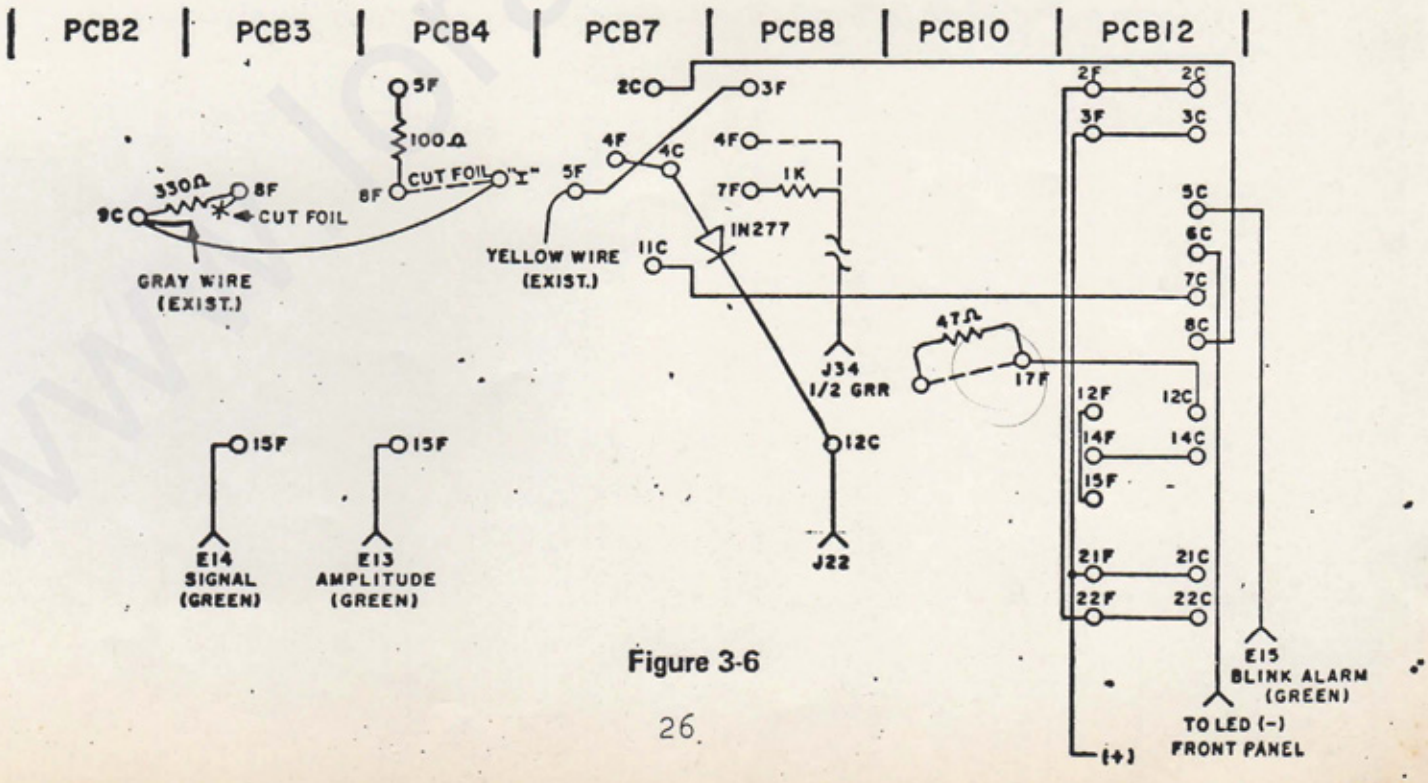
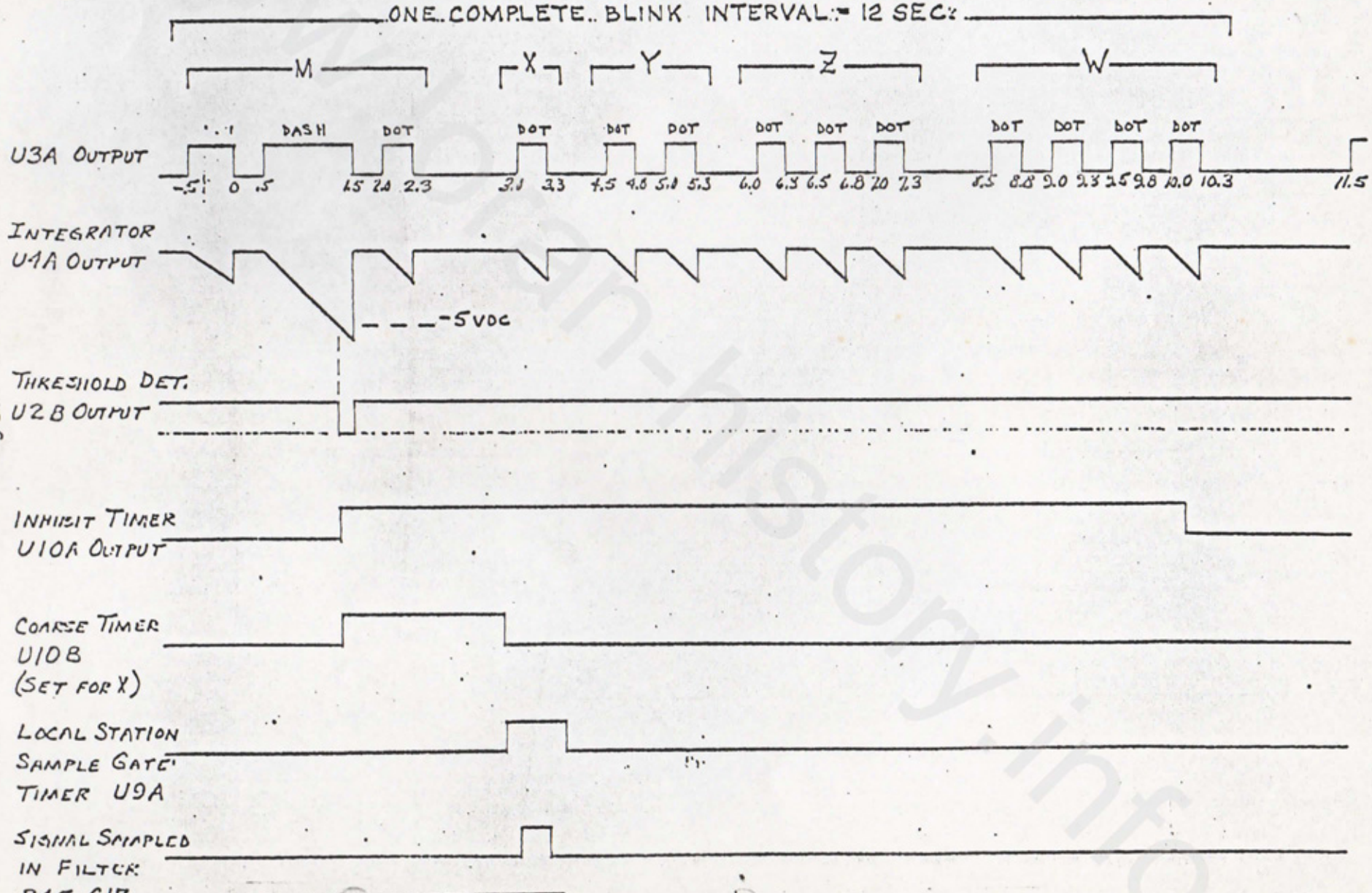


Figure 3-6

TABLE 2-I

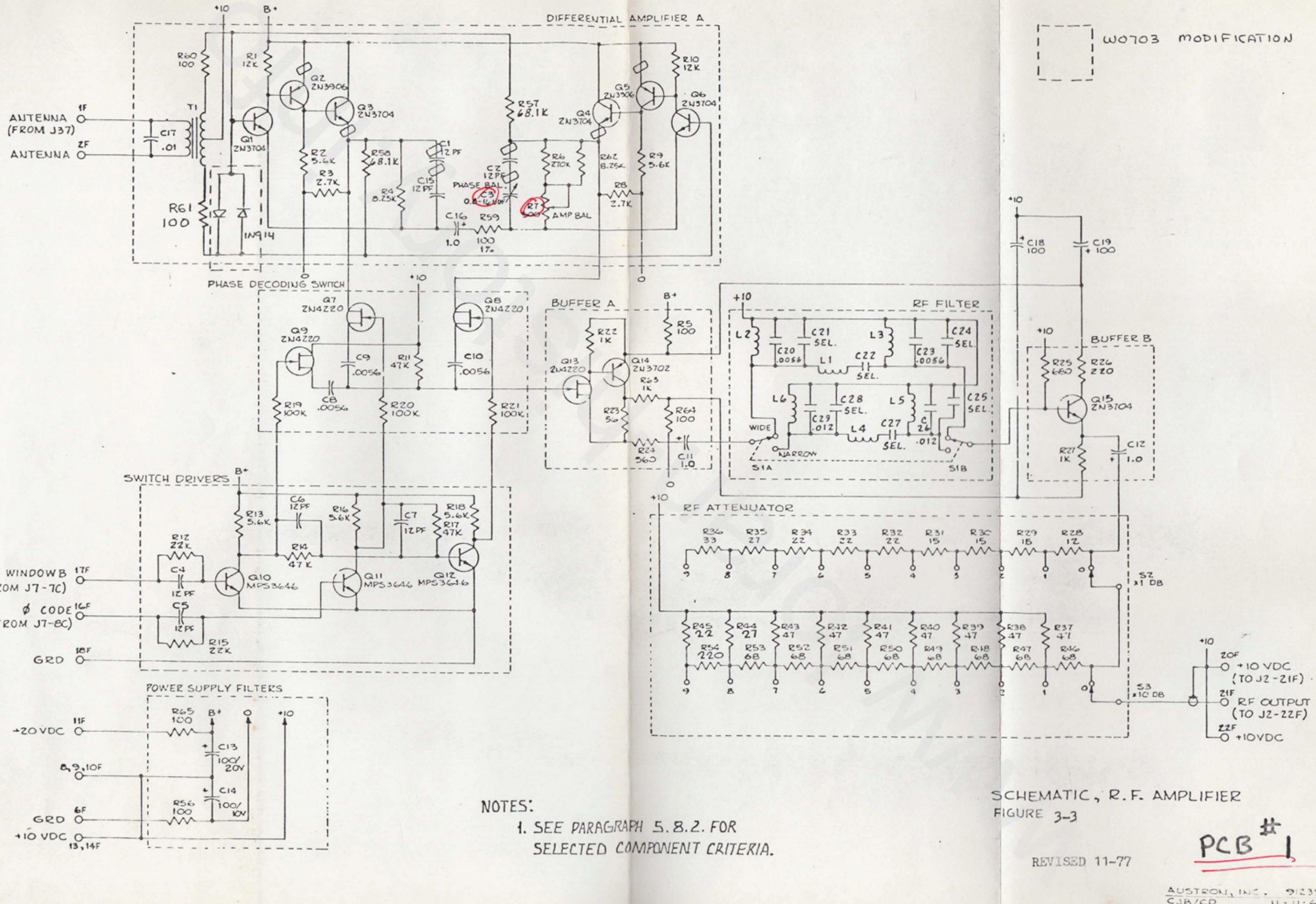
AUSTRON MODEL 2000CG LORAN-C
RECEIVER REAR PANEL MODIFICATIONS

	JACK	OLD LABEL	NEW LABEL	OLD TERMINATION	NEW TERMINATION
1.	J24	Phase Code	Start	J7-3C	J9-16F
2.	J23	1 kHz	Stop	J6-8C	J9-11F
3.	J22	10 kHz	X-Rate Blank Input	J6-9C	J8-12C
4.	J27	100 kHz	Freq. Std. Output 1 MHz	J6-10F	J9-3F
5.	J33	Ø Shifted 1 MHz	No Change	J6-11C	No Change
6.	J34	GRP	1/2 GRR	J8-4F	J8-7F
7.	E15 (New)	Blank	Blink Alarm	Blank	J12-5C
8.	E8	10 μs	M-LØ	J11-12F	No Change
9.	E7	100 μs	CORR	J11-10F	No Change
10.	E14 (New)	Blank	Signal (Green)	Blank	J3-15F
11.	E13 (New)	Blank	Amplitude (Green)	Blank	J4-15F
12.	J38 (New)	Blank	TPC	Blank	Pin A to J12-C19 Pin B to J12-C20 Pin C to J12-C7 Pin D to J12-C16 Pin E to J12-F10 Pin F to J12-F20 Pin G to 20 VDC Pin H to Gnd Pin I to J12-F19 Pin J – Vacant



TIME [illegible]DDER W0703-01 NIN[illegible] PULSE BLINK DETECTOR

Figure 3-2



NOTES:

1. SEE PARAGRAPH 5.8.2. FOR SELECTED COMPONENT CRITERIA.

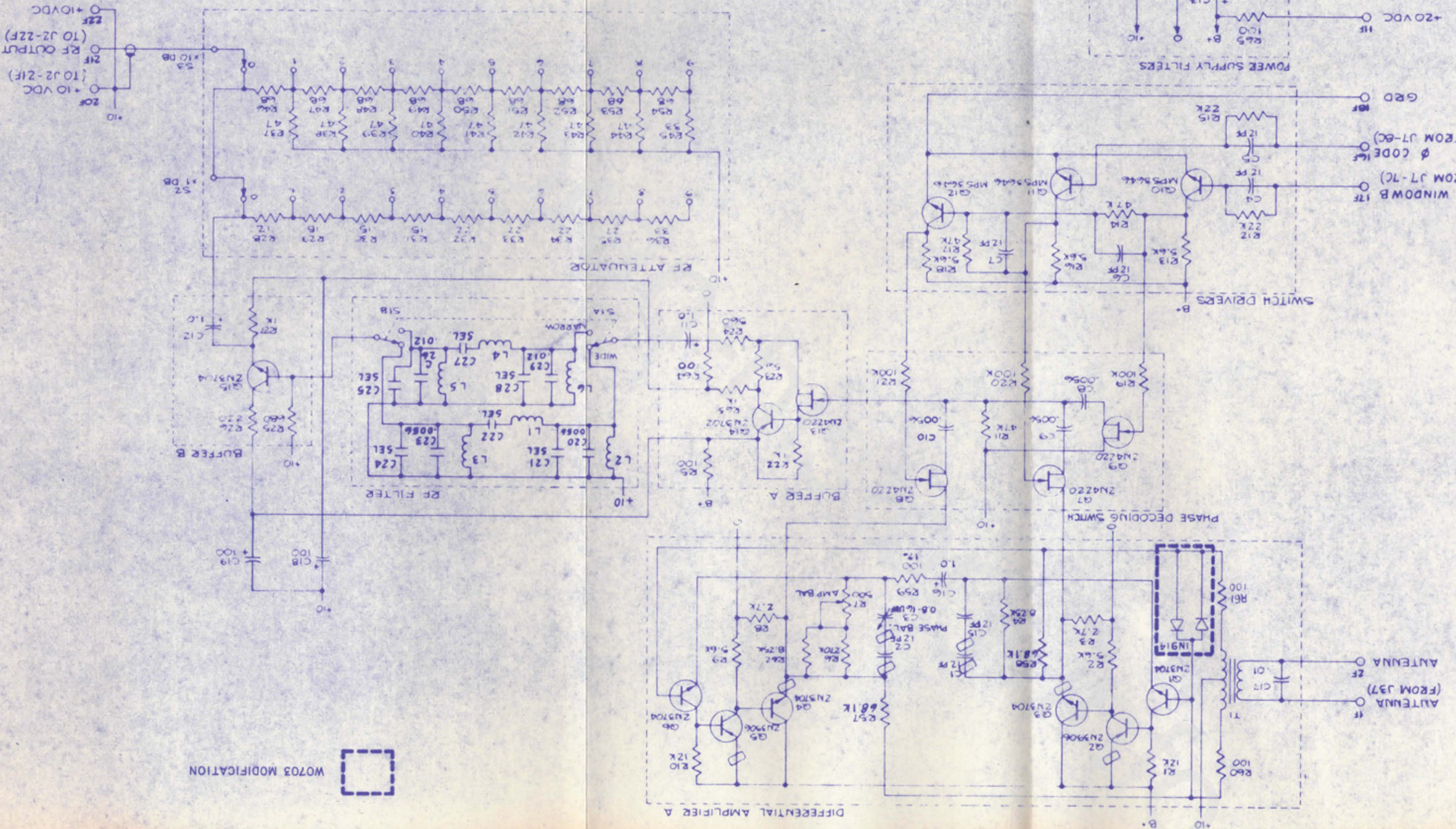
SCHEMATIC, R.F. AMPLIFIER
FIGURE 3-3

REVISED 11-77

PCB # 1

SCHEMATIC, R.F. AMPLIFIER

FIGURE 3-3



REVISED 9-14-72

(FROM J7-8F) GRP 3F O

W0703 MODIFICATION

Vcc

91A SN7474

7F 1K J34 GRP NOW LABELED 1/2 GRR

+20 VDC 1C6F +20

+5 VDC 21C6F +5 +5V FILTER C5 330 6VDC

GRD 22C6F

(FROM J7-17C) SCAN 1 KHz 17F

(FROM J9-20F) PHASE SHIFTED 1 MHz 20C

(FROM J3-15C) GRP SYNC 8F

DIVIDER A

INVERTER A

DIVIDER B

INVERTER B

INVERTER C

SIGNAL STROBE LOGIC

AMPLITUDE STROBE LOGIC

PHASE STROBE LOGIC

GATE A

RING COUNTER

GRP RESET CONTROL

LEAST SIGNIFICANT DIGIT GATE

GRP OUTPUT LOGIC

GRP OUTPUT BUFFER

GATE B

DIVIDER C

INVERTER E

DECODER

(FROM J3) LEAD/LAG 14C

(FROM J3-18F) AUTO CYCLE/CYCLE 2C

PART OF AMPLITUDE STROBE CYCLE

(FROM J2-16F, UNUSED) BLANKING 12C

(FROM J7-10C) BALANCE 10F

(FROM J3-13C) CYCLE/SCAN 15C

(FROM J3-19C) SIGNAL STROBE 19C

(FROM J7-11C) DEMODULATOR REFERENCE 11F

11C GRP 100 KHz (TO J6-11F, J9-11F)

19C GRP 2 KHz (TO J7-19C)

20C GRP 1 KHz (TO J7-20C, J9-16F)

12F GRP 500 Hz (TO J7-12C)

13F GRP 200 Hz (TO J7-13C)

14F GRP 100 Hz A (TO J7-14C)

15F GRP 100 Hz B (TO J7-15C)

18F GRP 10 KHz (TO J3-10C, J6-10F, J7-18C, J9-12F)

16F TENS GRP (TO J7-16C)

14C LEAST SIGNIFICANT DIGIT (TO J9-14F)

4F GRP OUTPUT (TO J34)

4C GRP (TO J3-4C)

13C AMPLITUDE STROBE (TO J4-6F)

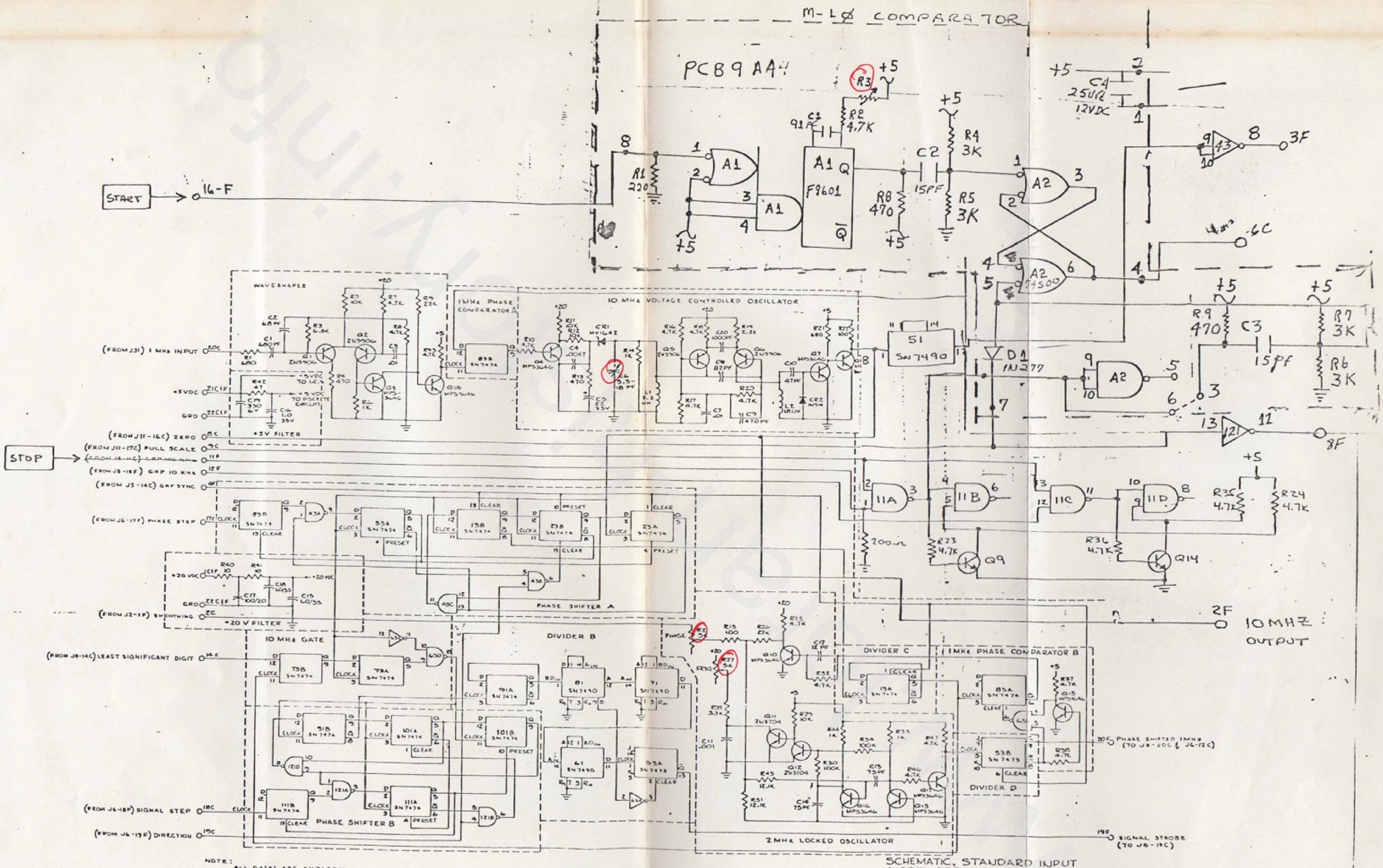
17C PHASE GATE (TO J2-7C, J4-17C)

18C SIGNAL/CYCLE STROBE (TO J3-6F, J7-18F)

NOTE: ALL INTEGRATED CIRCUIT PACKAGES ARE SN7400N UNLESS OTHERWISE SPECIFIED.

SCHEMATIC, GRP DIVIDER
MODEL 2000C
FIGURE 3-4

REVISED 11-77



SCHEMATIC, STANDARD INPUT
MODEL 2000C
FIGURE 3-5

REVISED 11-77

PCB #9

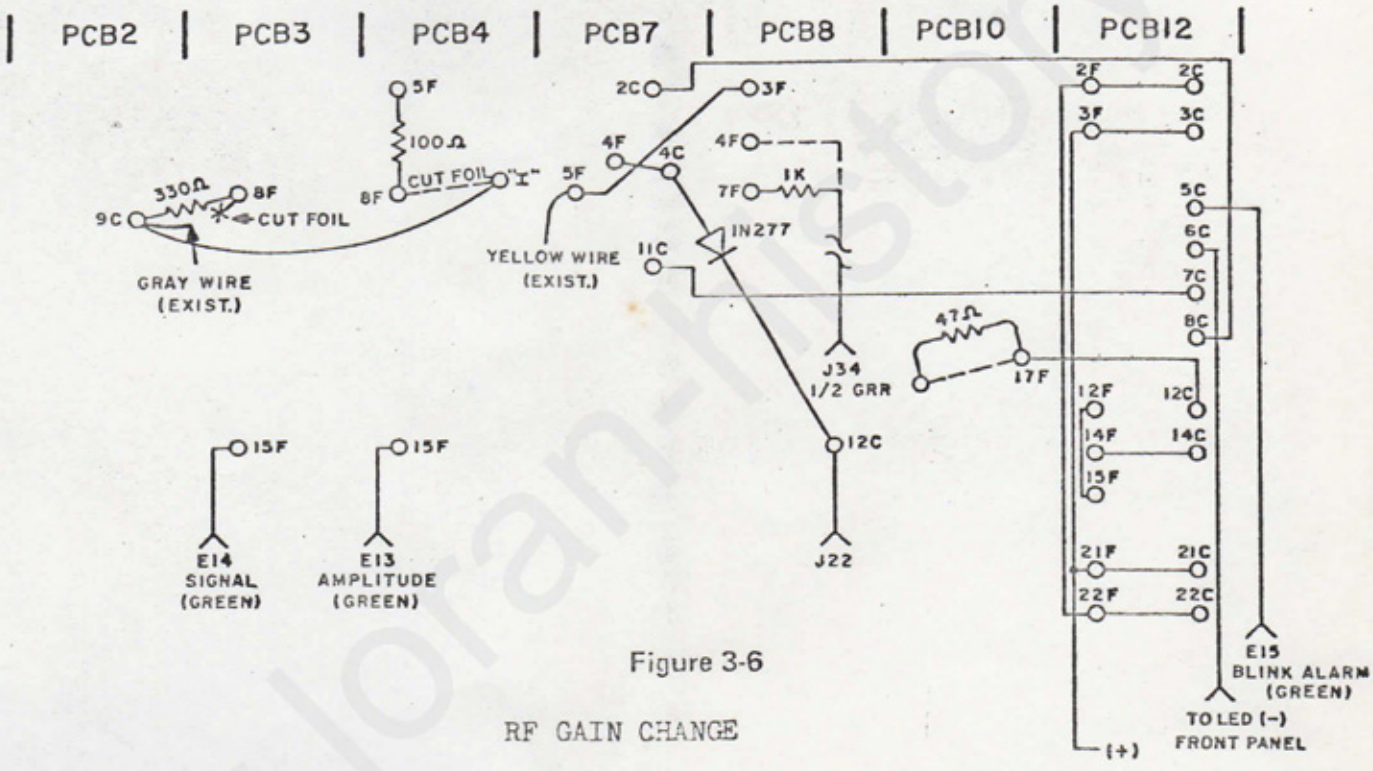
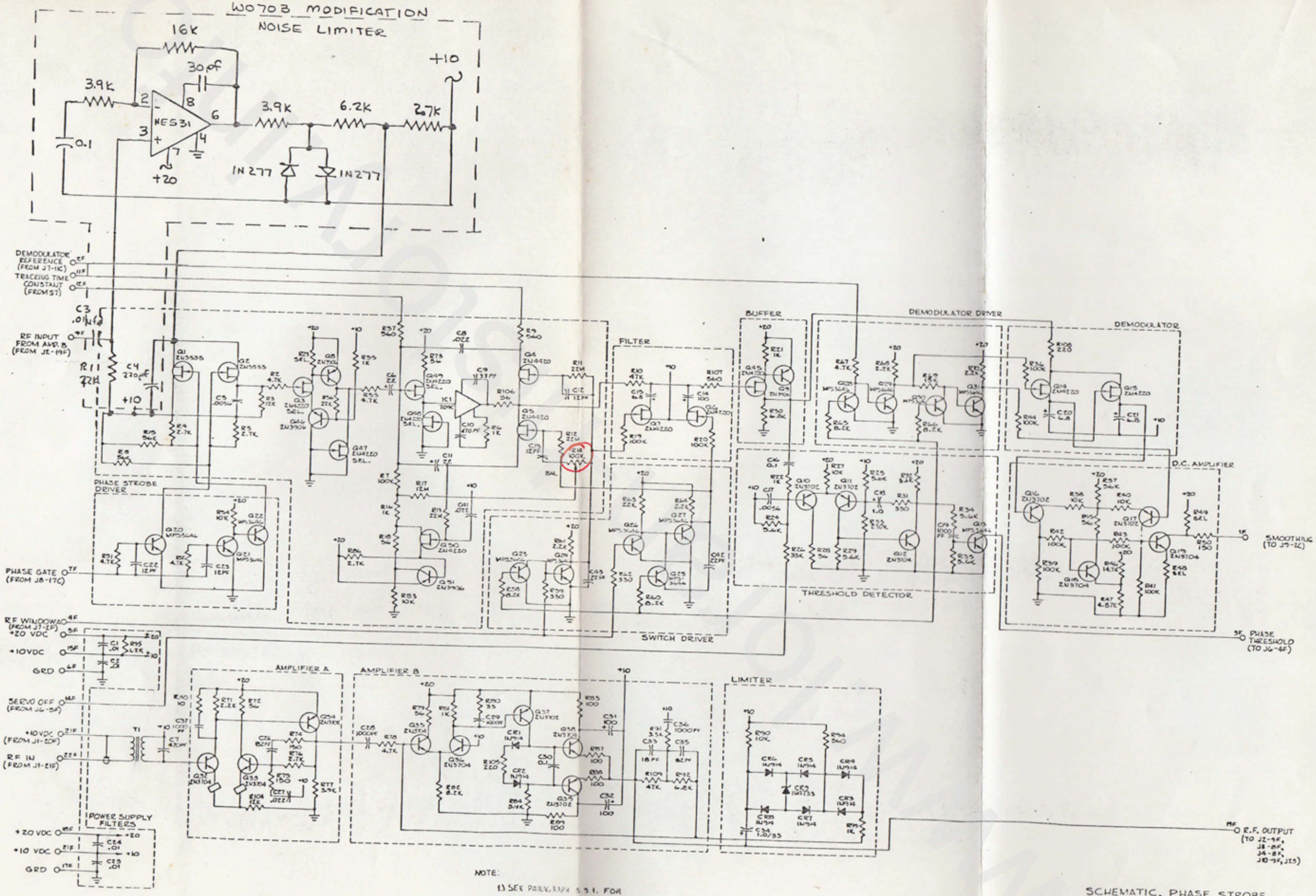


Figure 3-6

RF GAIN CHANGE



NOTE:

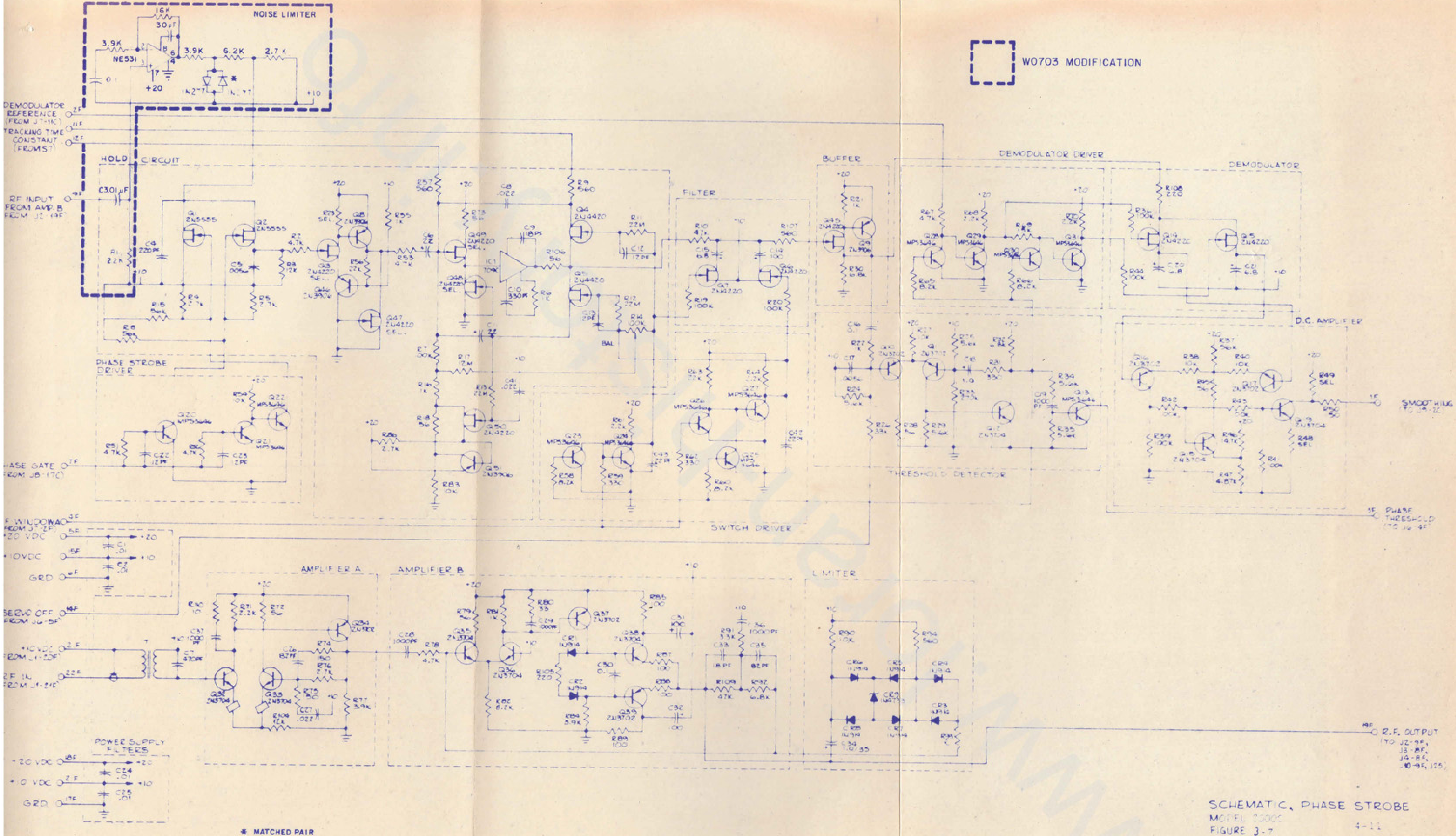
1) SEE PARAGRAPH 5.5.1. FOR SELECTED COMPONENT CRITERIA.

SCHEMATIC, PHASE STROBE
MODEL 2000C, 2004
FIGURE 3-7

AUSTRON, INC. 9280 C
CIR. CO 11-25-69

PCB #2

REVISED 11-77



SCHEMATIC, PHASE STROBE
MODEL 2000C
FIGURE 3-7
4-11

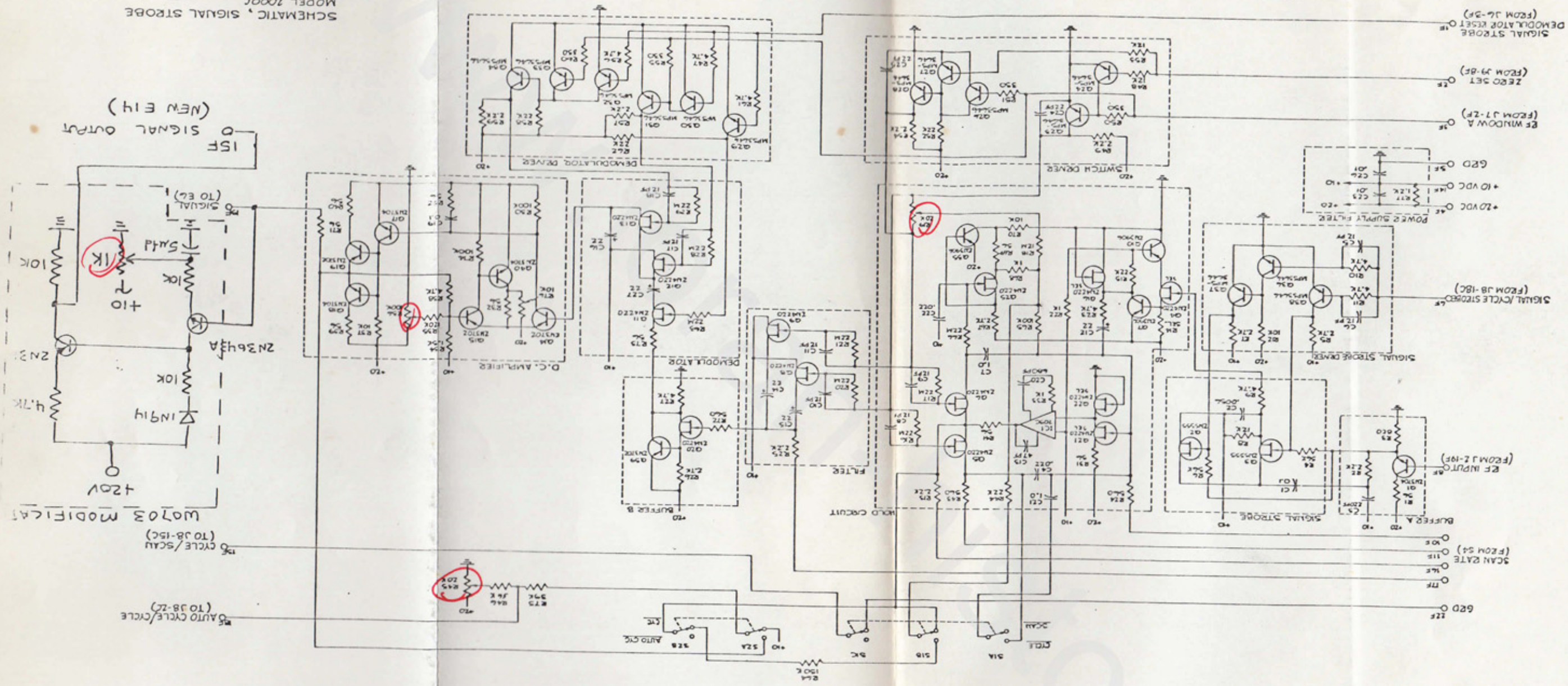
REV. 9-20-72
AUSTRON, INC. 9128C4
CJB/CD 1-25-69

SCHEMATIC, SIGNAL STROBE
MODEL 2000F
FIGURE 3-8

REVISED 11-77

NOTES:

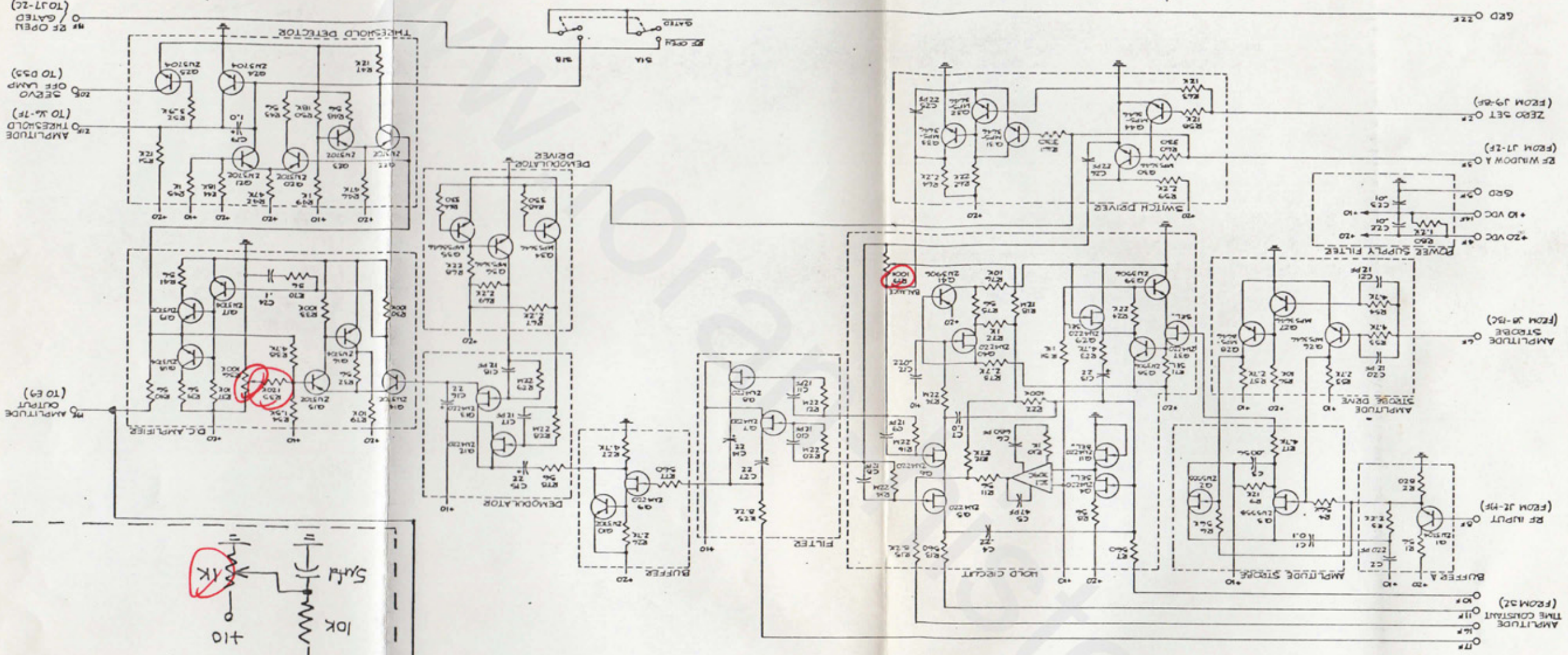
1. SEE PARAGRAPH 5.9.2 FOR SELECTED COMPONENT CRITERIA.

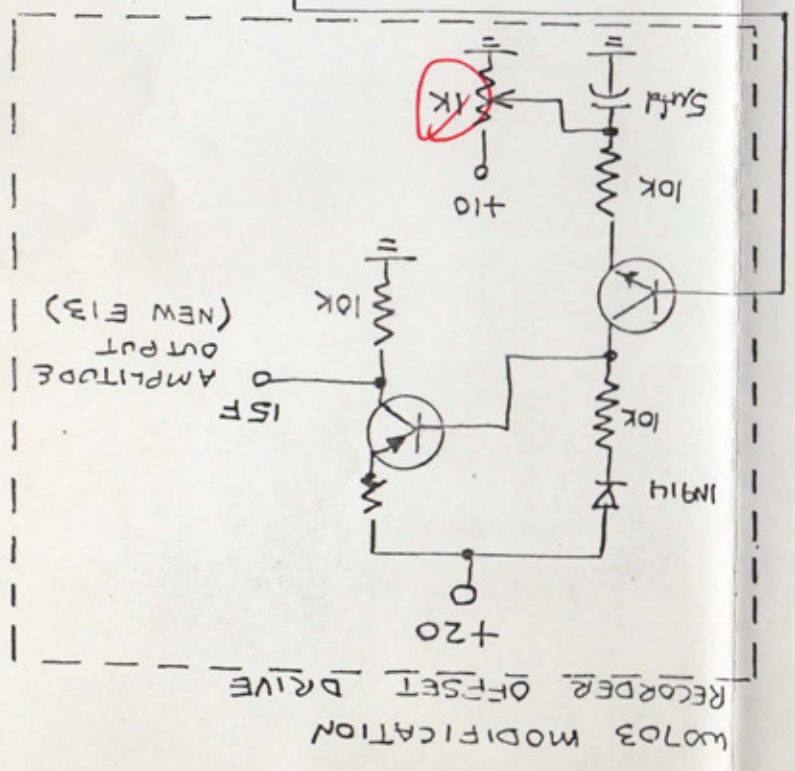


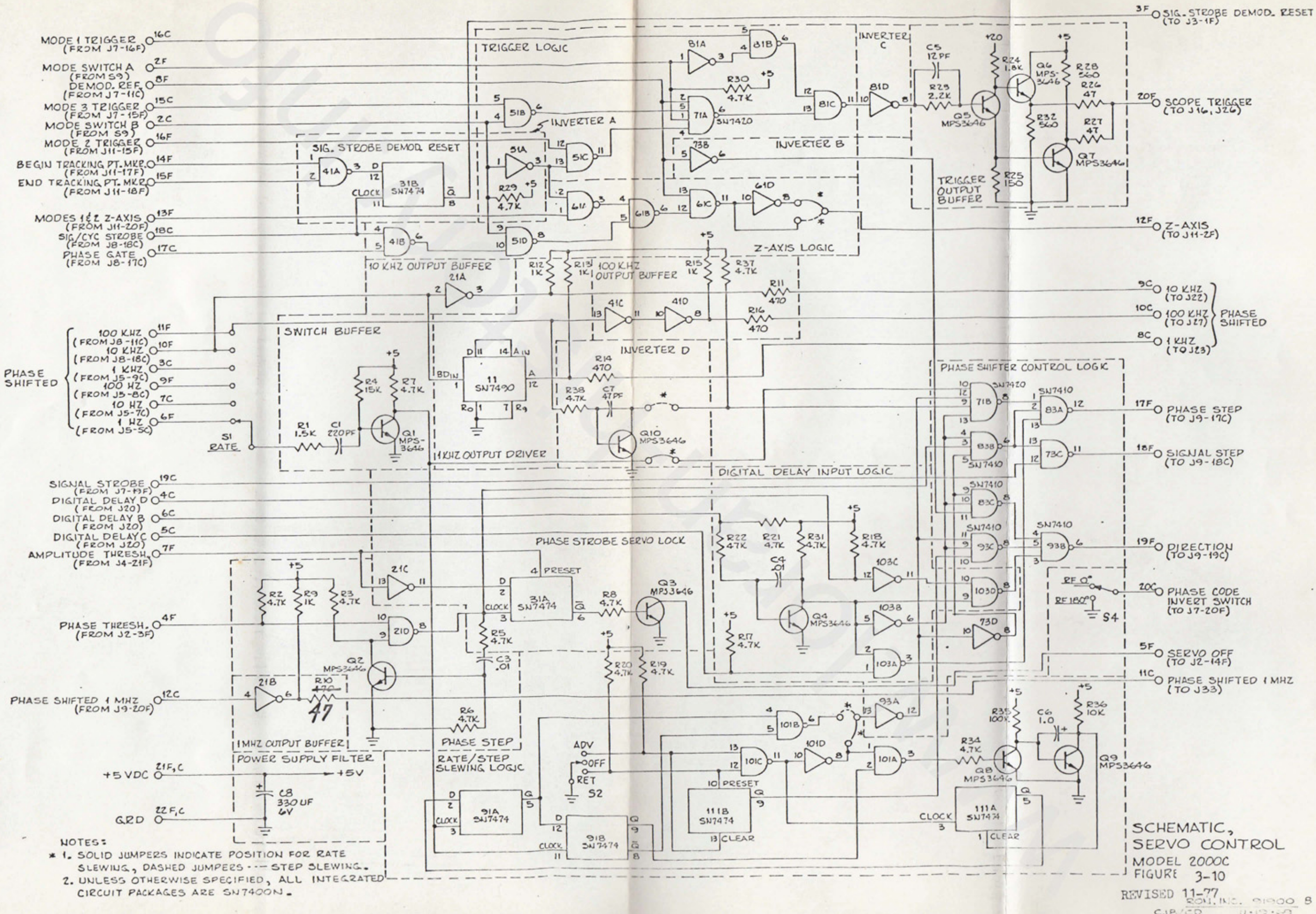
SCHEMATIC, AMPLITUDE STROBE
MODEL 2000C
FIGURE 3-9

REVISED 11-77

NOTES:
1. SEE PARAGRAPH 5.9.3 FOR SELECTED COMPONENT CRITERIA.



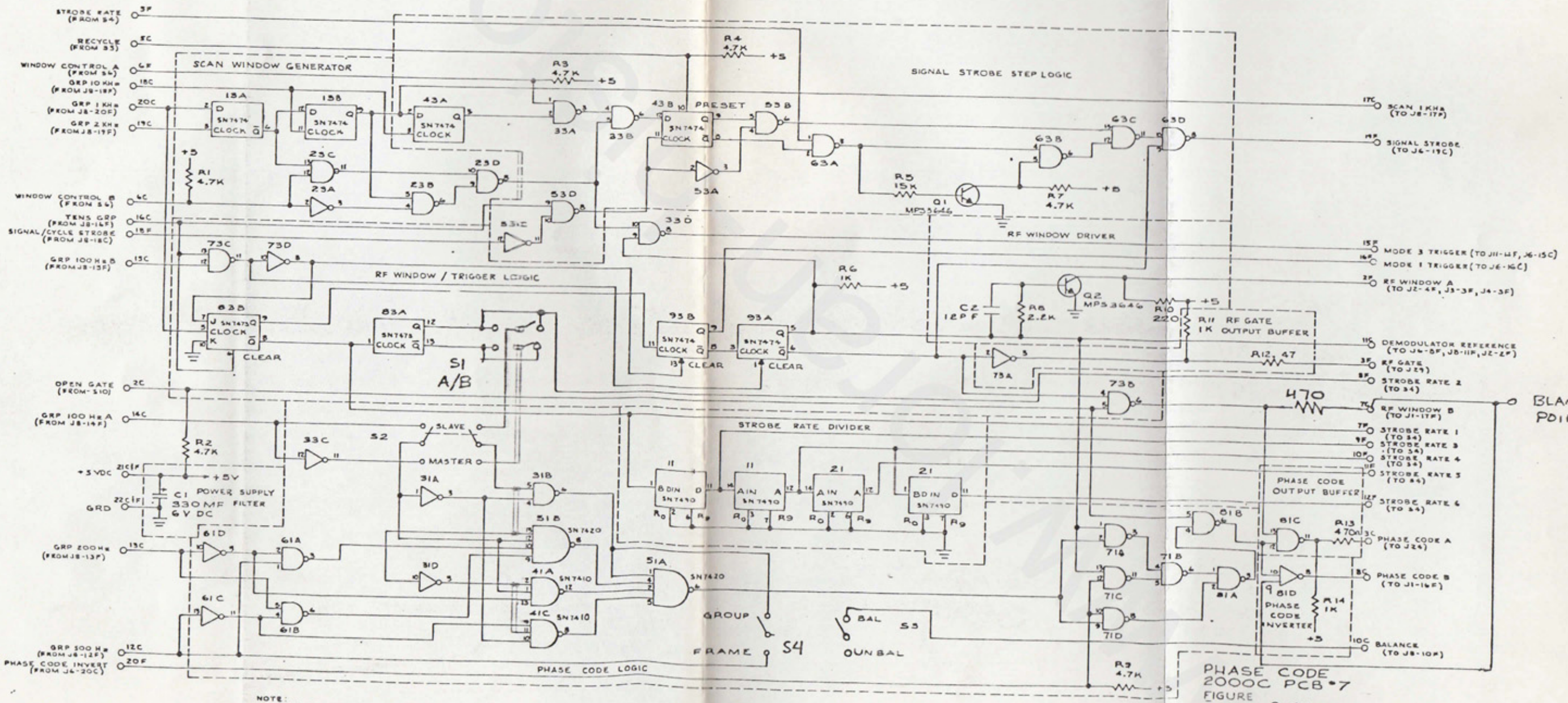



MODE 1 TRIGGER (FROM J7-16F)
MODE SWITCH A (FROM S9)
DEMOD. REF. (FROM J7-11C)
MODE 3 TRIGGER (FROM J7-15F)
MODE SWITCH B (FROM S9)
MODE 2 TRIGGER (FROM J11-15F)
BEGIN TRACKING PT. MKR. (FROM J11-17F)
END TRACKING PT. MKR. (FROM J11-18F)
MODES 1 & 2 Z-AXIS (FROM J11-20F)
SIG/CYC STROBE (FROM J8-18C)
PHASE GATE (FROM J8-17C)
TRIGGER LOGIC
INVERTER A
SIG. STROBE DEMOD RESET
INVERTER B
INVERTER C
TRIGGER OUTPUT BUFFER
SIG. STROBE DEMOD. RESET (TO J3-1F)
SCOPE TRIGGER (TO J16, J26)
Z-AXIS (TO J11-2F)
Z-AXIS LOGIC
10 KHZ OUTPUT BUFFER
100 KHZ OUTPUT BUFFER
INVERTER D
10 KHZ (TO J22)
100 KHZ (TO J27)
1 KHZ (TO J23)
PHASE SHIFTED
PHASE SHIFTED 100 KHZ (FROM J8-11C)
PHASE SHIFTED 10 KHZ (FROM J8-18C)
PHASE SHIFTED 1 KHZ (FROM J5-9C)
PHASE SHIFTED 100 HZ (FROM J5-8C)
PHASE SHIFTED 10 HZ (FROM J5-7C)
PHASE SHIFTED 1 HZ (FROM J5-5C)
S1 RATE
SWITCH BUFFER
1 KHZ OUTPUT DRIVER
DIGITAL DELAY INPUT LOGIC
PHASE SHIFTER CONTROL LOGIC
PHASE STEP (TO J9-17C)
SIGNAL STEP (TO J9-18C)
SIGNAL STROBE (FROM J7-13F)
DIGITAL DELAY D (FROM J20)
DIGITAL DELAY B (FROM J20)
DIGITAL DELAY C (FROM J20)
AMPLITUDE THRESH. (FROM J4-21F)
PHASE STROBE SERVO LOCK
DIRECTION (TO J9-19C)
PHASE CODE INVERT SWITCH (TO J7-20F)
S4
SERVO OFF (TO J2-14F)
PHASE SHIFTED 1 MHZ (TO J33)
PHASE THRESH. (FROM J2-3F)
PHASE SHIFTED 1 MHZ (FROM J9-20F)
1 MHZ OUTPUT BUFFER
POWER SUPPLY FILTER
PHASE STEP
RATE/STEP SLEWING LOGIC
ADV
OFF
RET
S2
+5 VDC (FROM J21F,C)
GRD (FROM J22F,C)
+5V
C8 330 UF 6V
NOTES:
* 1. SOLID JUMPERS INDICATE POSITION FOR RATE SLEWING, DASHED JUMPERS - - - STEP SLEWING.
2. UNLESS OTHERWISE SPECIFIED, ALL INTEGRATED CIRCUIT PACKAGES ARE SN7400N.
SCHEMATIC, SERVO CONTROL
MODEL 2000C
FIGURE 3-10
REVISED 11-77
CJB/CD

S1 A/B MODIFICATION

S4 MODIFICATION

BLANKING POINT MODIFICATION



NOTE:
UNLESS OTHERWISE SPECIFIED, ALL INTEGRATED CIRCUIT PACKAGES ARE SN7400N.

PHASE CODE 2000C PCB #7
FIGURE 3-11
REVISED 11-77

PCB #7

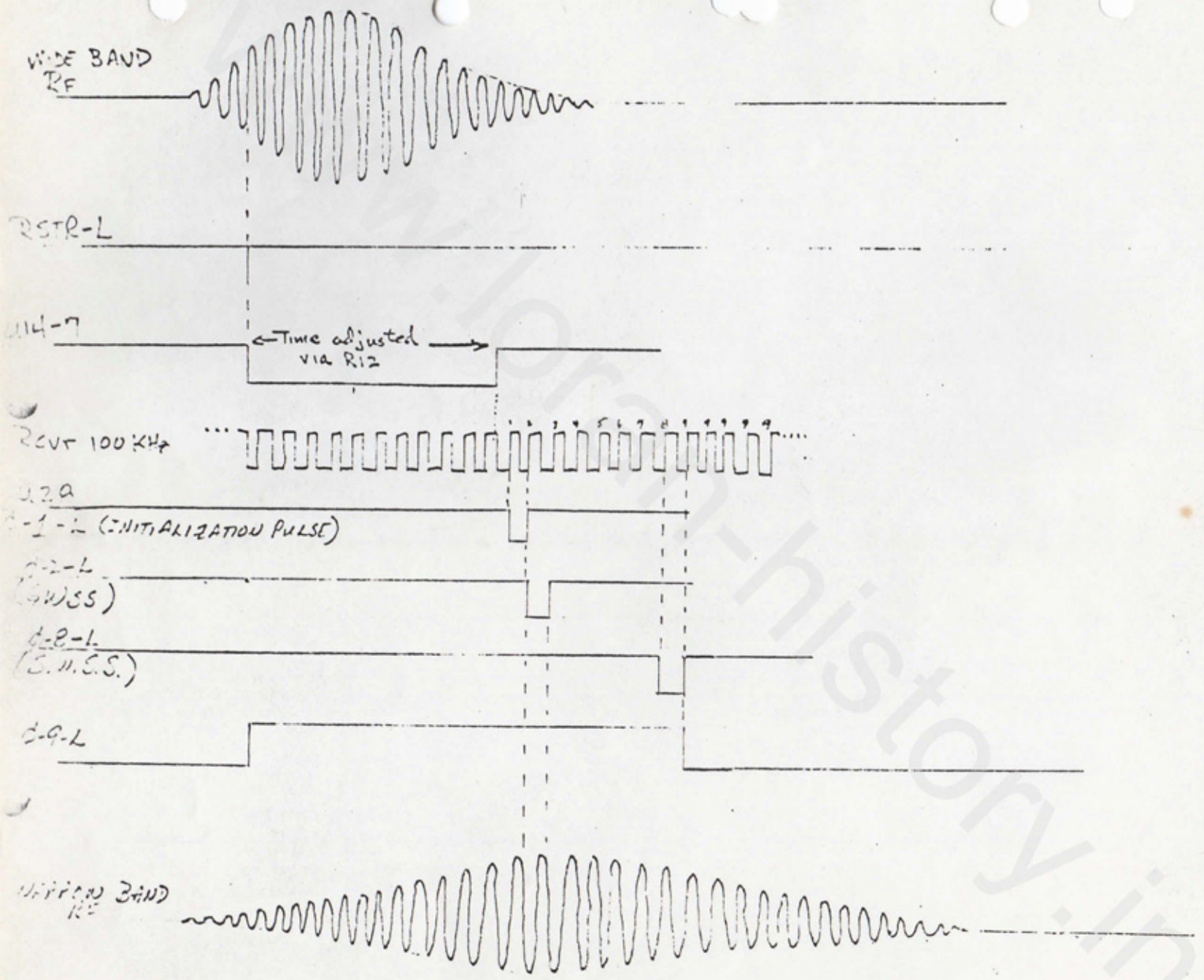
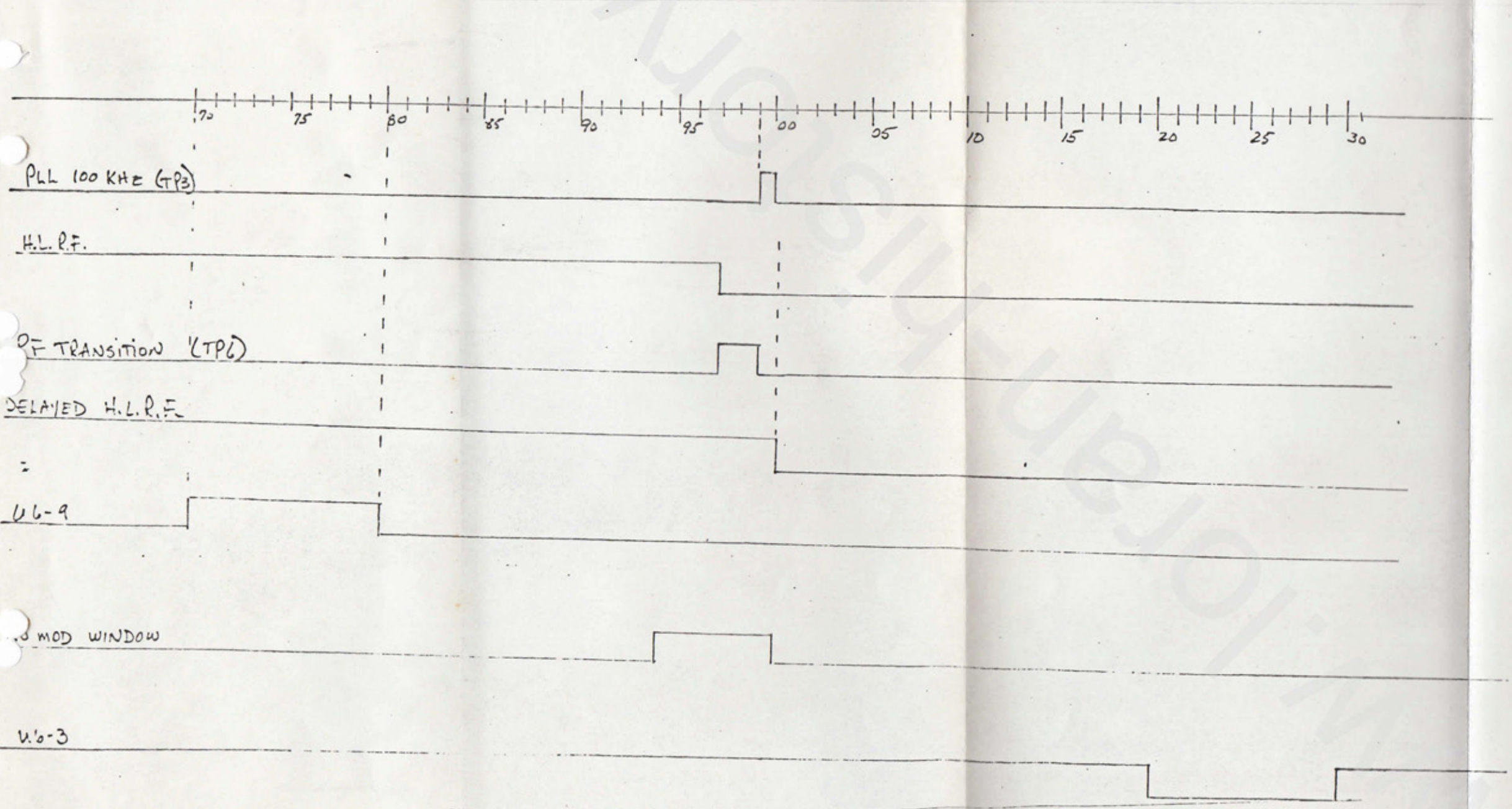


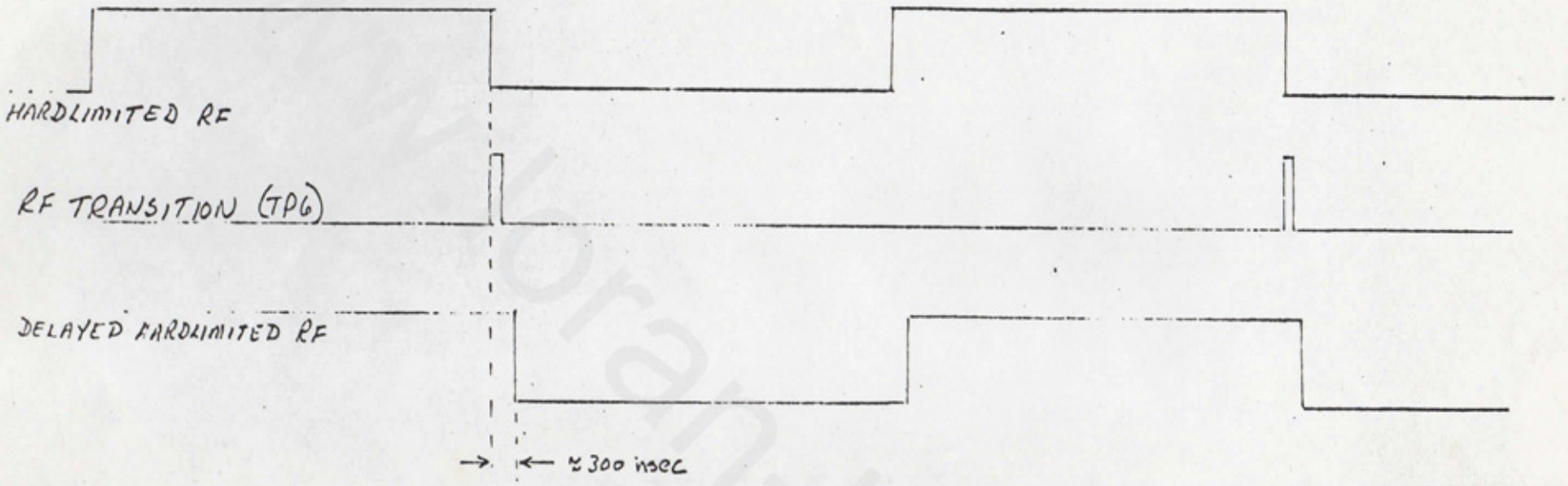
Figure 3-13

TIME LADDER DIAGRAM DIGITAL TIMING GENERATOR



TIME LADDER DIAGRAM PHASE LOCKED LOOPS AND LOOP SIGNAL MULTIPLEXER

Figure 3-14



OUTPUT OF SIGNAL LIMITER AND DETECTOR

FIGURE 3-15

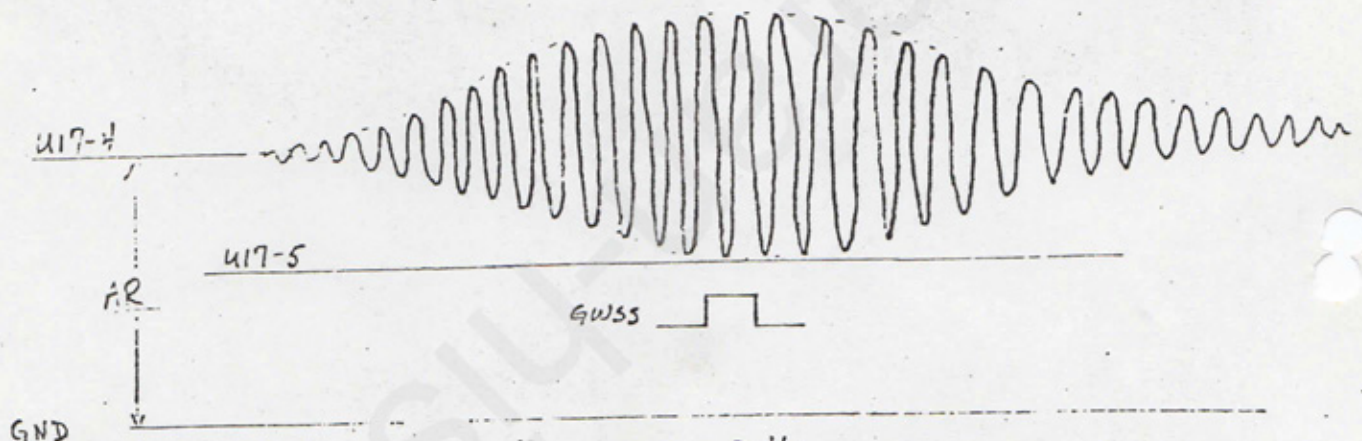
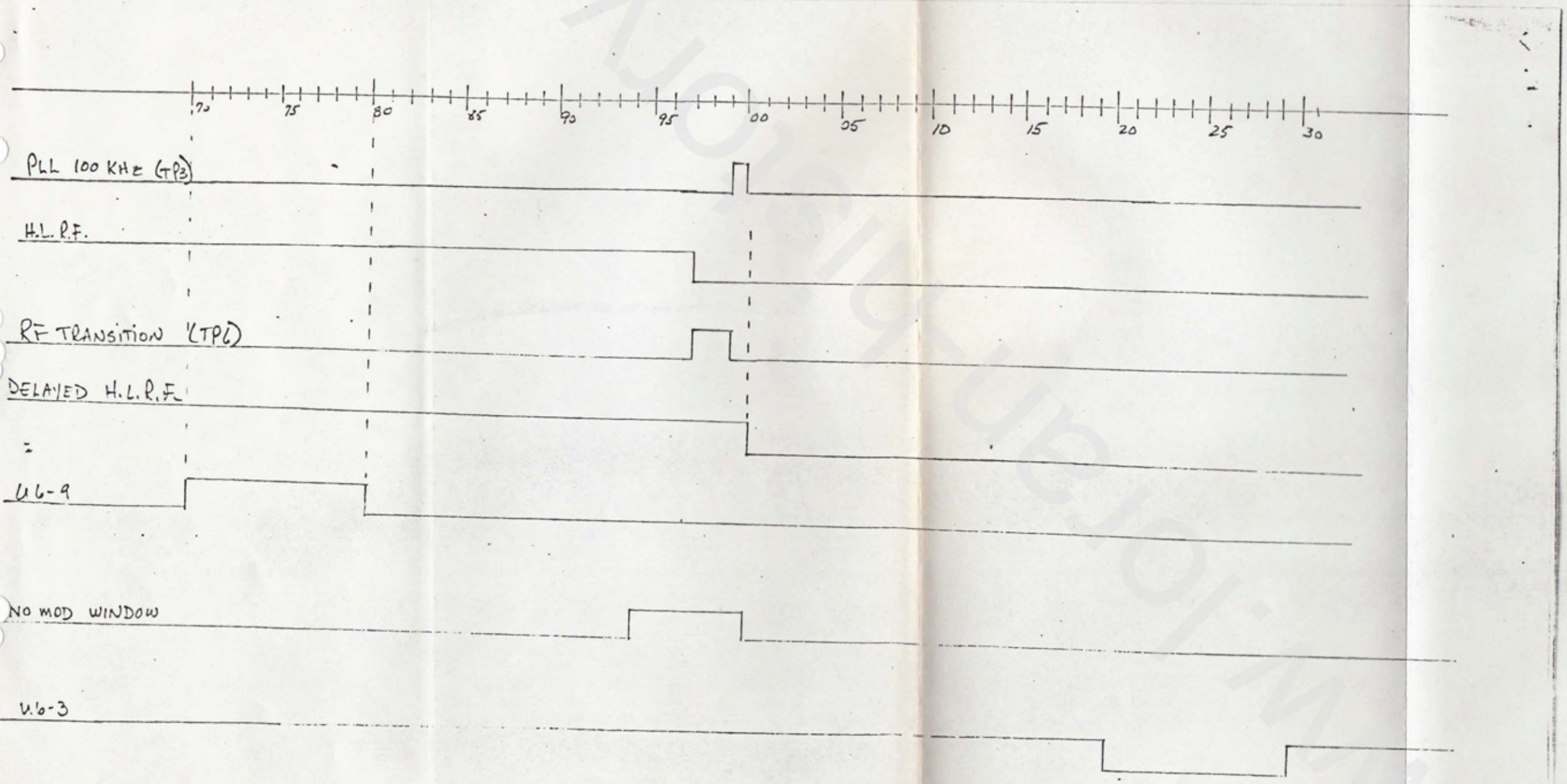


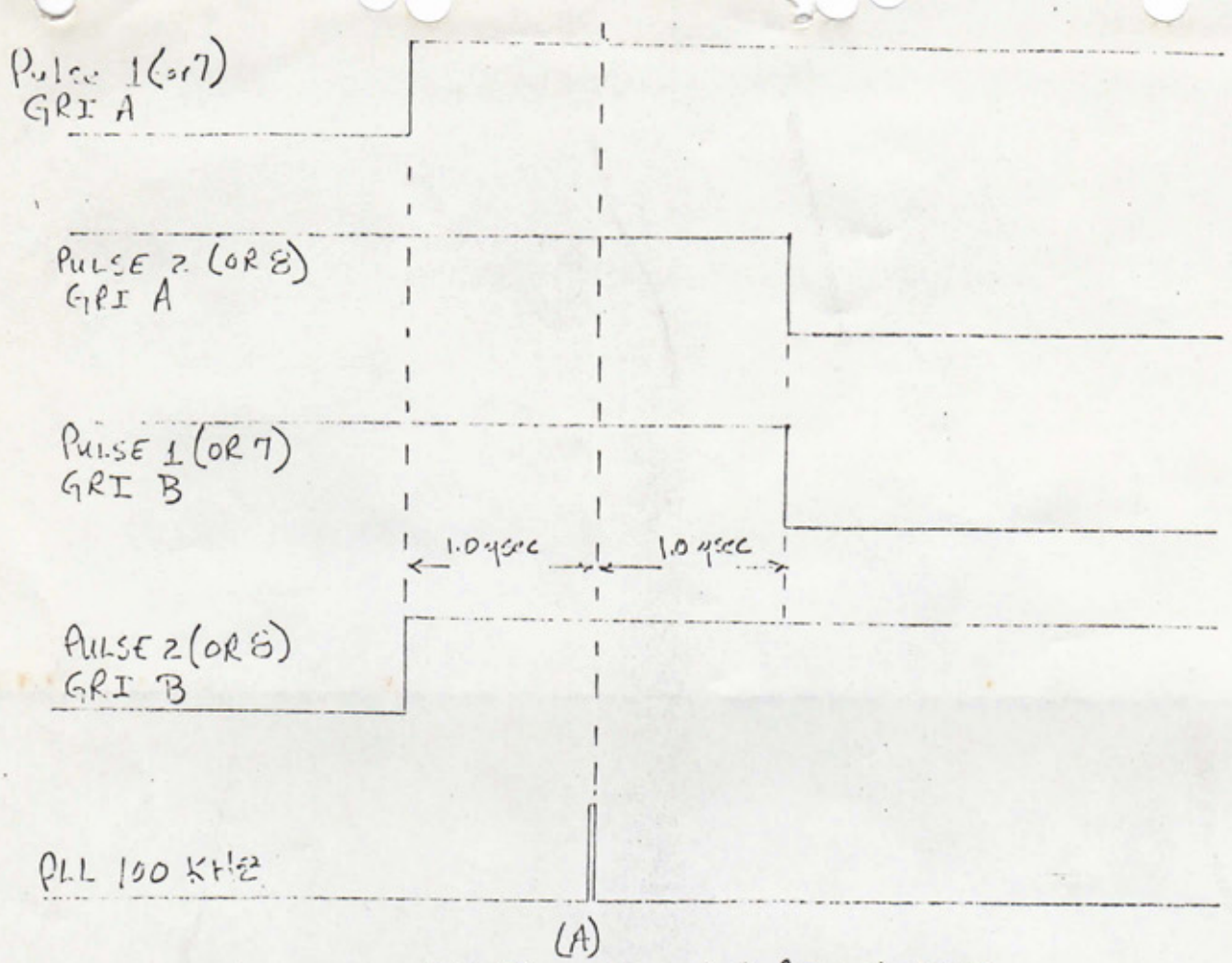
Figure 3-16

AMPLITUDE TRACKING INPUTS



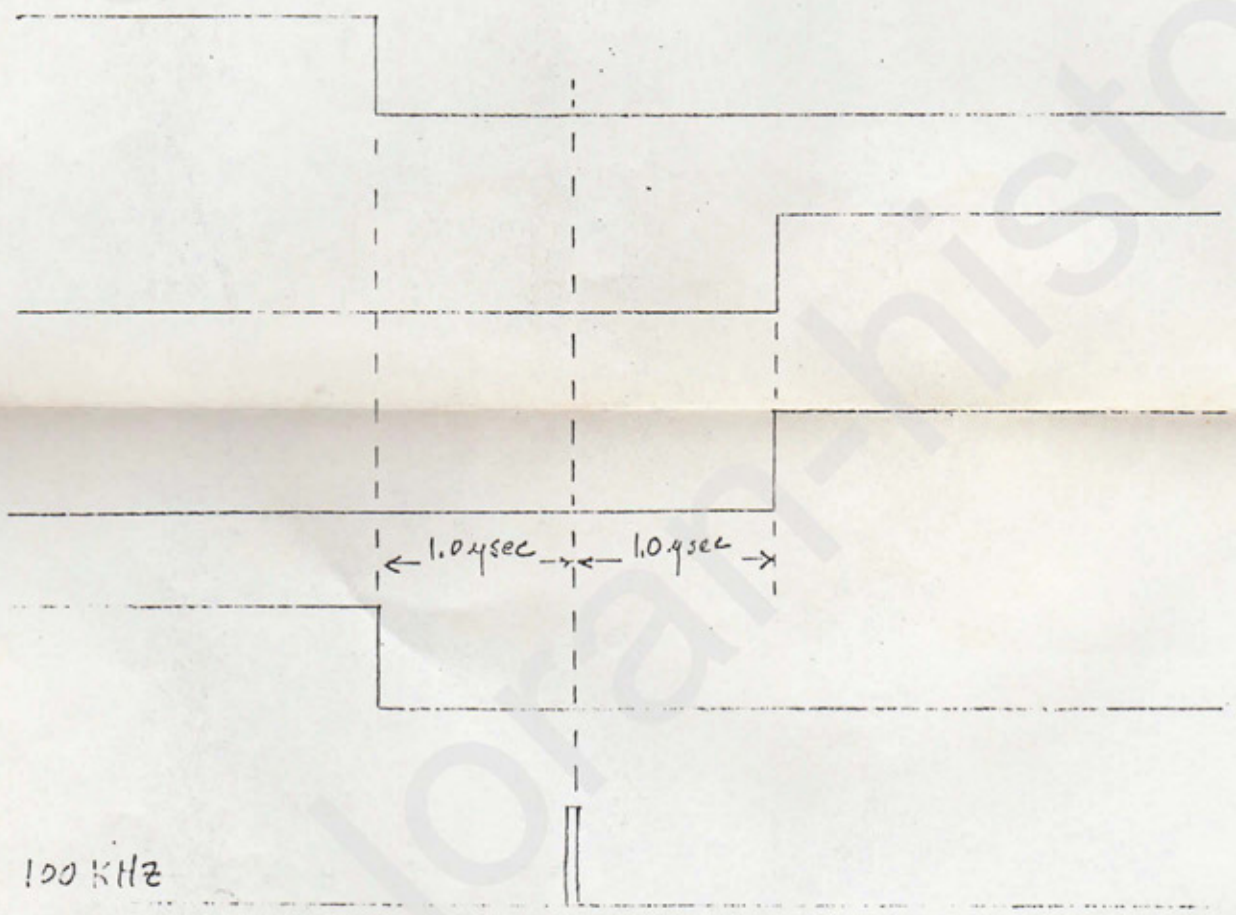
TIME LADDER DIAGRAM PHASE LOCKED LOOPS AND
LOOP SIGNAL MULTIPLEXER

Figure 3-17



(A)

Bi-Phase Decoded RF: 1 SENT

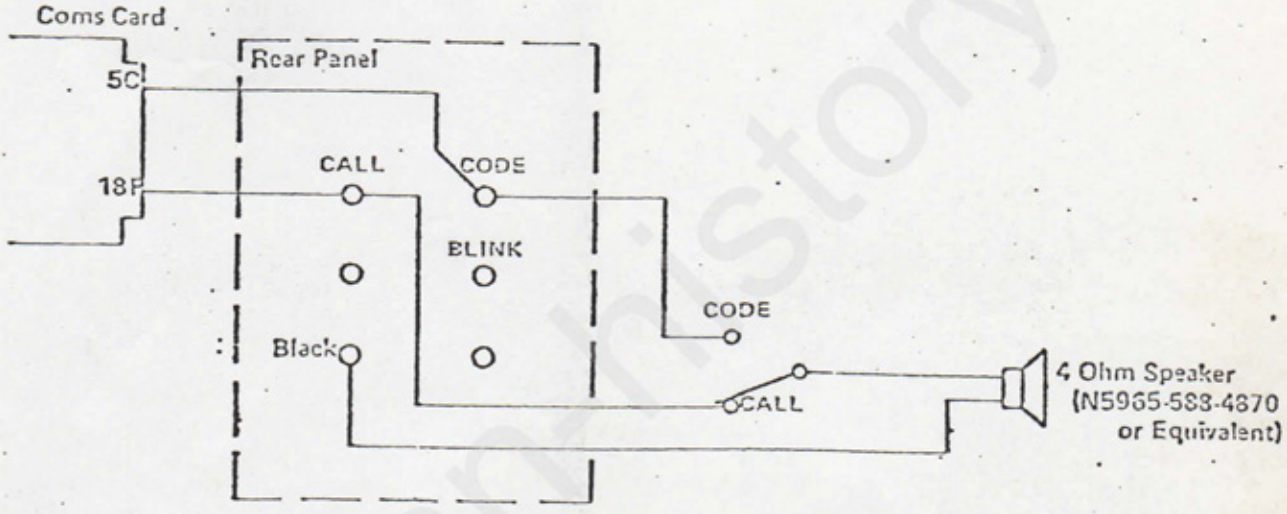


(B)

Bi-Phase Decoded RF: 0 SENT

BIT PHASE DETECTOR DECODED WAVEFORMS

Figure 3-18



CODE-CALL WIRING

FIGURE 4-1

CHASSIS CHANGES TO MODIFY

AUSTRON 2000C-1 TO A 2000C-2 RECEIVER

1. A new green binding post, jack E-16, has been added to the rear panel. It is labelled CALL and is internally connected to PCB12-18F. The Blink Alarm, jack E-15, has been relabelled to CODE and is internally connected to PCB12-5C.

OPERATING INSTRUCTIONS AND HOOKUP FOR

AUSTRON 2000C-2 RECEIVER

NINTH-PULSE COMMUNICATION PROVISION

1. The output of the Communication Blink card is available as a audio frequency signal at the rear panel binding posts labelled "CALL" and "CODE". The user should provide a SPDT switch and a 4 ohm speaker to connect to these outputs and ground, as shown below.

2. It is intended that the "CALL" output be monitored until the warbling signal is hear and then the speaker switched to the "CODE" output for the message. Upon the termination of the message, the speaker should be reconnected for the "CALL" function.