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ERRATA SHEET
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F.C. NO. 1 TYPE 1 TO CDFO-2000C RECEIVER

PURPOSE:

This Errata Sheet corrects the stock number for the CDFO-2000 Receiver Field Change Bulletin

PROCEDURE:

Apply a pen and ink correction to the ROUTINE INSTRUCTIONS and change the stock number from CG7610-01-GL7-6350 to CG7610-01-GE7-6350.

ROUTINE INSTRUCTIONS:

Upon completion, attach this Errata Sheet in front of the indicated field change in the applicable technical publications. Copies of this Errata Sheet may be obtained from Supply Center, Brooklyn using MILSTRIP procedures. NSN CG7610-01-GE7-6351 applies.

J.I. MALONEY, CAPT, USCG
CHIEF, ELECTRONICS SYSTEMS DIVISION

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COAST GUARD ADDENDUM

DRAFT

AUSTRON 2000C

VOLUME 1 OF2

NOVEMBER 1977

DRAFT

COAST GUARD ADDENDUM TO AUSTRON 2000C RECEIVER TECHNICAL MANUAL

VOLUME 1 TABLE OF CONTENTS

SECTION

COAST GUARD ADDENDUM TO AUSTRON RECEIVER TECHNICAL MANUAL

1.0 INTRODUCTION

The Austron 2000C Timing Receiver has been modified for use at Coast Guard Loran Transmitting Stations as a backup control receiver. These modifications do not effect in any way the basic performance or method of operation of the receiver. Rather they effect the peripheral capabilities and outputs of the receiver to optimize them for use at loran stations. These modifications do not impair its use as a timing receiver, and in fact, improve it somewhat in providing a greater resolution phase comparator readout. In providing this improved resolution, the 10 μs meter indication is no longer useful for slewing one or more cycles. Proper use of the Time Interval Counter (Paragraph 2.5.3) can substitute for the original meter indication. In section two, basic operating and installation instructions for the modified input and outputs of the receiver are presented, and in section three a more complete theory of operation and the electrical schematics for the modifications are given. The schematics of the modification are provided for continuity with a complete schematic description of the basic receiver provided in the Austron Technical Manual. Field personnel should follow the directives governing field maintenance, module exchange, and basic repair philosophy for the receiver (see Section 4.0).

2.0 INSTALLATION AND OPERATION

Throughout the following discussion, all inputs and outputs which are discussed as logic levels are TTL compatible. That is, they require TTL type "current sinking" inputs and the outputs drive TTL loads.

2,1 MASTER NINTH PULSE BLINK DETECTOR

The master ninth pulse blink detector is an entirely automatic circuit which is located on card number 12 in the far left card slot of the receiver. The blink detector uses the internally amplified RF signal being tracked by the receiver, (the output of the 5 kHz "viewing filter") and the receiver's internal RF Gate timing waveform. Its only interaction with the receiver is to turn on the receiver's RF channel during the period that the master's ninth pulse is present, after the normal eight pulse group. The detection of Master blink at the local station is displayed via a red light emitting diode (LED) on the front panel, and is available as a logic level at the

rear panel binding post labeled BLINK. The blink detector automatically adjusts the detection threshold for the noise level of the remote signal. The method of adjustment is known as CONSTANT FALSE ALARM RATE (CFAR) and operates reliably down to -6 dB Signal-to-Noise ratio. This ratio is defined in the conventional Loran-C manner (relative to the sampling point) and measured at the receiver's antenna terminal in a 30 kHz bandwidth. The blink detector effectively samples the output of the 5 kHz viewing filter during a period from 40 μsec before the peak of the ground wave signal component to 60 μsec after the peak. In this manner it automatically takes advantage of additional first hop skywave energy. When the SNR drops below the point at which the module can detect blink (either due to an increase in noise level or major cancellation of the filter output because of groundwave/skywave cancellation) a blink alarm is generated. Thus a false blink alarm is always indicative of a loss of ninth pulse blink detection capability. The SNR conditions required for this loss of detection are reached after an observer can no longer discern the Loran-C pulses (groundwave and skywave) among the noise in the receiver's VERTICAL output with the mode switch in position "2". The time required to detect ninth pulse blink is approximately 1.5 minutes, although this will vary somewhat with the type and level of noise interference. The detector is essentially immune to cross-rate interference.

There is no light or horn drive available to repeat the ninth pulse code because the CFAR technique sets the detection

threshold for each individual ninth pulse at a level that results in a large number (about 30 percent) of incorrect decisions when the ninth pulse is absent. Later synchronous averaging removes these short term errors and provides the essentially false alarm free detection capability (when the SNR is above the minimum required value).

To program the master ninth pulse blink detector board a jumper wire is soldered between the pin labeled C and one of the four pins labeled X, Y, Z, W, according to the designation of the local station as X, Y, Z, or W. THIS PROGRAMMING MUST BE DONE ON THE STATION SINCE THE RECEIVER IS SHIPPED WITHOUT STATION PROGRAMMING. The logic output at the rear panel is capable of driving four TTL loads, approximately 6 mA. A low logic level is a local blink alarm.

2.1.1 The ninth pulse blink detector should be checked once a week for proper operation. To do this, take from the standby TD-989 Timer the output of TP-4 of W-486-6/BLINK board (P card) and connect it to TP-6, blue test point on PCB 12 of timing receiver. "Blink" the standby timer by selecting your station designation on the front panel and note when the blink alarm LED turns on. The time to recognize blink should generally

be between 1-2 minutes. After the test, stop blink and remove jumper connections between test points. FAILURE TO DO THIS WILL DISABLE THE TIMING RECEIVER'S CAPABILITY OF RECOGNIZING ON-AIR MASTER BLINK.

2.1.2 If the noise conditions at the station are generally severe it may be advisable to lengthen the time to detect blink. This should cut down the number of false alarms. To increase the time to recognize blink to 4-12 minutes, the value of resistor R45 can be increased by a factor of two or three. This will not be accomplished unless directed by COCO.

2.2 RF PROTECTION

The RF input amplifier is protected, by back-to-back diodes, from damage due to overloads caused by the local station's signal. This overload protection applies to either a signal on the rate being tracked, or, in the case of a double rated station, the local crossing-rate signal. These diodes, in the case of crossing-rate signals, only protect the input RF amplifier from damage. The cross rate blanking input must be used as detailed in the next paragraph to eliminate errors due to the local cross-rate signal.

2.3 CROSS-RATE BLANKING

Tracking errors introduced by a local cross-rate signal are eliminated by connecting a cross-rate blanking

signal to the rear panel input labeled CROSS-RATE INPUT. This input, which utilizes a sampling inhibit line available within the receiver, inhibits track strobe sampling during the cross-rate period and closes the receiver's RF GATE. A logic low at the rear panel input causes these two responses. For normal installations this input may be directly connected to the AN/FPN-54 Loran-C Timer, LOCAL INTERVAL OUTPUT, available at the rear of the Control Unit. For more sophisticated applications, additional cross-rate blanking to eliminate errors caused by remote cross-rate signals can be accomplished by using diodes to logically combine other sources of cross-rate blanking, as shown in Figure 2-1.

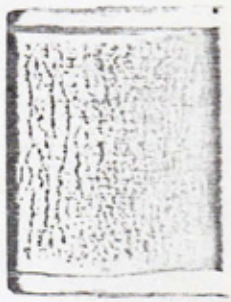
2.4 1/2 GRR OUTPUT

A 1/2 GRR logic waveform is available at the receiver's rear panel at the jack labeled 1/2 GRR. This waveform is retimed via a modification within the receiver to the accuracy of the receiver track strobe. It is provided for use with a time interval counter for generating a precise time-difference. This time-difference can be a remote signal to local signal time-difference (using the 1/2 GRR available at the C-8621/FPN Timer Set Control) or a remote-to-remote time-difference using a second timing receiver's 1/2 GRR output. Either transition of the 1/2 GRR waveform may be used, each transition has the resolution and precision of the receiver's tracking strobe. Use of a cross-rate blanker with the receiver will cause the 1/2 GRR time-difference to change during the period the blanking waveform overlaps the receiver's 1/2 GRR waveform transitions.

2.5 INTERNAL START-STOP PHASE COMPARATOR

2.5.1 The two phase comparators of the unmodified timing receiver, which provided a 0 to 10 and 0 to 100 μs phase comparison have been removed, and replaced by a single phase comparator in which both inputs to the comparator are brought out to the rear panel. In principal, any two periodic, logic level waveforms of the same frequency may be phase compared with this circuit, although most Coast Guard applications will utilize 1

MHz waveforms; thus providing a 0 to 1 μs phase or time-difference measurement. The start-stop definition of the phase comparator inputs are shown in Figure 2-2. The average value of this waveform, the phase comparison output, is available at a rear panel binding post and displayed on the front panel meter. As can be seen from this figure, a time retard of the stop input will increase the duty cycle of the phase comparison pulse, and result in an increase in the average value displayed on the meter, and available at the rear panel chart recorder drive. The zero and full-scale test switch on card 11 of the receiver affects the start-stop phase comparator exactly as described in the Austron Technical Manual for the original phase comparator.



2.5.1.1 The phase comparator is attached as a piggy-back board to PCB 9 and must be aligned on-station, after the receiver is locked to the desired signal, the preceding steps taken, and a time interval counter connected as in paragraph 2.5.4. Alignment of the phase comparator is accomplished by securing power to the receiver, opening the right hand front door, removing PCB 9, and placing it on the extender.

Power should be reapplied and the receiver locked onto the desired signal for a period of at least 15 minutes before attempting phase comparator adjustment. When the receiver has achieved lock and settled, the mid-scale potentiometer (located on the piggy-back, Figure 2-3) should be adjusted for mid-scale deflection on the front panel meter. This meter reading and recorder pen position is now calibrated to the tenths microsecond reading occurring on time interval counter. This reading should be logged for future use as a correlated number for that receiver. If a mid-scale deflection cannot be obtained, secure receiver power, remove PCB 9 from the extender. Locate the jumper connected between terminals 3 and 6 on the piggy-back board (Figure 2-3). Disconnect the jumper from terminal 6 and reconnect to terminal 5; reinstall the board and carry out the preceding alignment procedure. When all adjustments are complete, remove power, and replace PCB 9 in its normal slot for operation. The recorder and front panel meter are now calibrated for mid-scale indication of the time interval counter time difference reading.

2.5.2 Phase Comparator Installation Instructions

2.5.2.1 Remote-To-Local

To measure the time difference bewteen a remote signal (nominally the master when at a secondary station), connect the Ø SHIFTED 1 MHz output from the timing receiver rear panel to the START INPUT of the phase comparator and connect the AN/FPN-54 1 MHz output (this is the OPERATE 1 MHz available at the rear of the FPN-54 Timer Set Control) to the STOP INPUT. Since the local signal phase is locked by the cycle compensation servo loop to the OPERATE 1 MHz time base within the FPN-54 Timer Set, the timing receiver's front panel meter will now read MASTER MINUS LOCAL time-difference on a 0-1 μs full scale basis.

2.5.2.2 Remote-to-Remote

To generate a normal loran time-difference phase track when two timing receivers are used to track two remote signals, connect the PHASE SHIFTED 1 MHz output from the timing receiver tracking the Master to the START INPUT of the secondary tracking timing receiver, and connect the PHASE SHIFTED 1 MHz from the secondary-tracking receiver to the STOP INPUT of the secondary-tracking receiver's phase comparator.

2.5.3 Timing Receiver Application

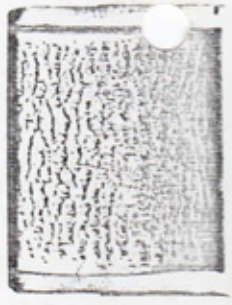
To operate the modified Austron Timing Receiver as a conventional timing receiver, connect the TIMING RECEIVERS FREQUENCY STANDARD 1 MHz output (this is only a logic compatible version of the frequency standard input sinewave) to the START INPUT and connect the receiver's PHASE SHIFTED 1 MHz output to the STOP INPUT. This configuration provides an oscillator-to-remote, 0 to 1 μs phase comparison. The addition of a time interval counter, using either a 1 PPS OUTPUT TICK from the oscillator clock or a TOC SYNCHRONIZED TRIGGER and the 1/2 GRR output provides an accurate and unambiguous representation of the time of emission, as seen at the receiver's location, of the remote Loran-C signal.

2.5.4 Phase Comparator Chart Recorder Connection

To connect the phase comparator output to a voltage type recorder (e.g., Brush AN/GSH-18) connect a 3 kΩ resistor (any value between 2.7 k and 3.3 k is satisfactory) between the M-LØ OUTPUT binding post and the Black or ground binding post. Connect the recorder across this resistor. For a current type recorder (e.g., Texas Instruments AN/USH-8) connect the recorder directly to the output and ground binding posts without the parallel 3 kΩ resistor.

To calibrate the recorder, place the ZERO/F.S. switch on printed circuit card 11 in the ZERO position and mechanically zero the recorder pen (do not use the recorder's zero switch). Place the zero/F.S. switch in the F.S. position and adjust the potentiometer on card 11 labeled "10 μs" until the recorder pen indicates full scale.

The front panel meter readout of the phase comparator is calibrated at the factory and should not require field adjustment. This adjustment can be performed (card 11 must be placed on an extender board) by following the instructions in the Austron Technical Manual.



2.5.4 Phase Comparator Chart Recorder Connection

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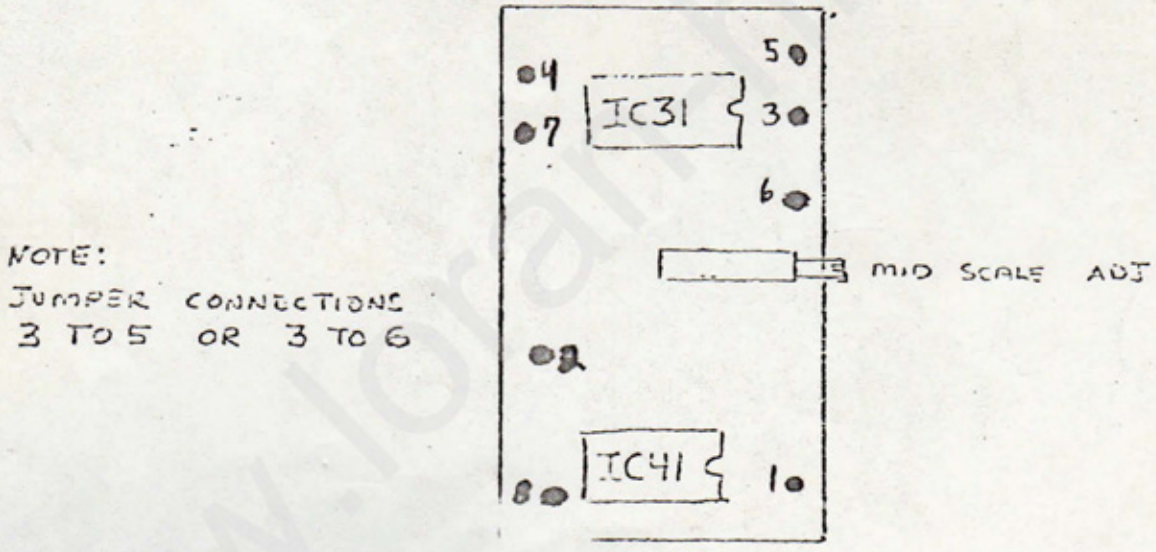

FIG 2-4

ONE MICROSECOUND PHASE COMPARATOR

The phase comparator is attached as a piggy-back board to PCB 9 and must be aligned on-station, after the receiver is locked to the desired signal, the preceeding steps taken, and a time interval counter connected as in paragrapn 2.5.4. Alignment of the phase comparator is accomplished by securing power to the receiver, opening the right hand front door, removing PCB 9, and placing it on the extender.

Power should be reapplied and the receiver locked onto the desired signal for a period of at least 15 minutes before attempting phase comparator adjustment. When the receiver has achieved lock and settled, the mid-scale potentiometer (located on the piggy-back, Figure 2-4) should be adjusted for mid-scale deflection on the front panel meter. This meter reading and recorder pen position is now calibrated to the tenths microsecond reading occurring on time interval counter. This reading should be logged for future use as a correlated number for that receiver. If a mid-scale deflection cannot be obtained, secure receiver power, remove PCB 9 from the extender. Locate the jumper connected between terminals 3 and 6 on the piggy-back board (Figure 2-4). Disconnect the jumper from terminal 6 and reconnect to terminal 5; reinstall the board and carry out the preceeding alignment procedure. When all adjustments are complete, remove power, and replace PCB 9 in its normal slot for operation. The recorder and front panel meter are now calibrated for mid-scale indication of the time interval counter time difference reading.

2.6 RECEIVER RF GAIN AND SERVO τ

The internal level of the RF signal of the timing receiver used by the viewing filter and phase tracking loop has been increased +12 dB over that specified by the manufacturer. This produces no changes in the front panel indications or the amplitude set point of the front panel meter nor any receiver alignments. Its only performance manifestations is a reduction of approximately 1/2 in the SERVO τ shown on the front panel switch. The purpose of this change was to eliminate the errors which might be introduced by ground loops in the generally high CW RF environment of a Loran-C ground station timer room.

2.7 NOISE LIMITER

The Austron receiver has a built-in noise limiter (PCB #2); however it is set at approximately +38 dB (accounting for the 12 dB loss described in Section 2.6) and this is too wide a dynamic range for typical Loran-C ground station applications where notch filters remove CW interference, and atmospheric or burst noise is the most serious remaining interference. A diode type noise limiter, functionally identical to that used in the AN/SPN-30 receiver and AN/FPN-46 Timer, has been installed ahead of the phase strobe sampling gate. It limits signal excursions to approximately 3 dB greater than the amplitude of the RF cycle peak occurring directly after the RF

zero crossing being tracked. Since the limiter is only on this card it has no effect on any of the other amplitude sampling circuits nor on any of the manufacturer's alignment instructions.

2.8 SIGNAL AND AMPLITUDE CHART RECORDER OUTPUTS

The analog processing circuitry which generates the SIGNAL (CYCLE/SCAN) information and AMPLITUDE outputs, and meter displays, is referenced to analog receiver ground of +10 volts. When the receiver is used with voltage type recorders, such as the Brush AN/GSH-18, the result is unsatisfactory because the changing component of the signal output is on the order of ± 1 volt, about the 10 volt analog ground offset. To correct this, an offset circuit has been added to PCB 3 and 4 to provide a recorder drive signal whose offset is approximately 2 volts with variations of ± 1.5 volts.

2.8.1 Connection to Current Type Recorder

Insure that both inputs to the recorder are isolated from timer room ground. Connect one to the white or + 10 VOLT binding post, and the other, via an approximate 2-3 kΩ rheostat, to either the SIGNAL or AMPLITUDE red binding post.

For the SIGNAL readout, place the receiver's control in SCAN, depress the SCAN restart pushbutton and center the recorder pen when the panel meter reads mid-scale zero. When the Loran-C pulse scan takes place, adjust the rheostat added above for the desired recorder deflection. For the AMPLITUDE readout, attenuate the input RF signal until the receiver loses lock and the panel meter settles at mid-scale zero. Adjust the recorder pen to the chart edge, relock the receiver and adjust the rheostat added above for a mid-scale recorder reading.

2.8.2 Connection to Voltage Type Recorder

Connect a voltage recorder input between a black binding post (ground) and the green SIGNAL or AMPLITUDE binding posts. For the SIGNAL readout, zero the recorder with the input OFF, then depress the SCAN restart pushbutton and when the meter indicates mid-scale use the recorder's variable potentiometer (attenuator set to .05 volts/line) to center the pen at recorder mid-scale. Since the recorder is unipolar, it is not possible to change the ratio of this mid-scale offset to dynamic signal component, this is factory set by the recorder drive modification. For the AMPLITUDE recorder output, zero the recorder with the input OFF and then with the receiver tracking at the normal sampling point adjust the recorder gain for a mid-scale recorder deflection.

2.8.3 Use of the SIGNAL and AMPLITUDE Recorder Tracks

The SIGNAL track (draw-out of the received Loran-C pulse) in the SCAN position is used during initial lock-on, as described in the Austron Technical Manual. Use of this feature for third-cycle identification should be performed at the direction of COCO or other suitable authority. It can be displayed several times per day as part of a normal watch routine. The CYCLE data, present at the recorder output when the auto cycle/cycle switch and the cycle scan switch are in the cycle, cycle positions respectively could more properly be labeled "envelope index voltage". The CYCLE ZERO potentiometer on PCB#3 should be adjusted during initial receiver installation to zero this readout at mid-scale on the remote signal being tracked (after the third cycle tracking point has been identified). Later shifts in the remote signal Envelope-to Cycle Difference (ECD) will be observable in this readout. Most important, it can form an important aid to relocking the receiver if the local time reference has been lost and hence a REMOTE-LOCAL time difference using ½ GRR waveforms cannot be formed. To do this, slew the receiver until the approximate third cycle tracking point can be

seen on the wideband RF display. After the receiver has locked onto this zero crossing, depress the ZERO switch (PCB #11) for 30 seconds, or until the envelope index output (CYCLE) has returned to zero. If, upon release of the ZERO switch, the envelope index begins to rise, the receiver is sampling too far back into the pulse. Jump the receiver 10 μs and repeat the above procedure, until the index voltage shows no immediate tendency to change, which signifies return to the previously used signal tracking point. In the case where the timing receiver is being used to control a remote secondary station, the same technique can be used to correct 10 μs jumps in that signal. In this application however, the receiver should remain fixed in time (constant time-difference with respect to the local FPN-54 1/2 GRR or remote master 1/2 GRR) and the index readout set to zero with the "ZERO" switch on PCB-11 then observed for tendency. Corrective action in this case is to move the remote signal until the index voltage does not change rapidly after zeroing. Fine-adjust LPAs can then be issued based on the time difference and phase track. The AMPLITUDE output also provides very useful information for either of the cases discussed above (providing the receiver's attenuator is not changed) and this signal responds more quickly than the envelope index (CYCLE) readout. However, due to the fact that the remote signal amplitude can change due to transmitter adjustments (and often does during chain "crisis" conditions) the amplitude output is often not satisfactory to make the final $\pm$ 10 μs adjustment. It is also sensitive to

amplitude perturbations caused by skywave, which the envelope index output will of course reveal. In the case of gross skywave errors such as locking onto the leading edge of the skywave, the envelope index will indicate correctly but the amplitude readout will indicate an extremely large signal. Thus together, providing the remainder of the receiver controls are not readjusted, they can provide a rapid relock to the remote signal when the local time reference is lost or the remote signal is grossly out-of-time.

2.9 TIMING RECEIVER OPERATING TECHNIQUES

2.9.1 A Time-of-Arrival Receiver

The most important concept to keep in mind when using the Austron Timing Receiver as a backup Loran-C control receiver is that the final control data Master Minus Local time-difference) is based on a receiver that measures only time-of-arrival (TOA). While a time-difference is formed from this TOA measurement through use of the AN/FPN-54 information, it is not a time-difference in the generally used Loran-C sense because both signals do not travel through the same processing path, as they do in a timer's receiver for example. Thus any change in the receiver's path or any change in the relationship of the FPN-54 time base (1 MHz) to the radiated signal will cause an apparent change in time-difference which did not in fact occur. In practical terms this means that

care must be used so that receiver parameters are not unknowingly changed and one must be aware of when changes in the FPN-54 system might result in apparent time-difference changes that should in fact be discounted in comparing past data with present.

The following is a representative list of equipment changes that might be reflected in a change of apparent time-difference:

2.9.1.1 Receiver

a. Change of notch filter tuning. (On many receivers this has been disabled.)

b. Change in length of antenna input line or termination (remember that if the timer-s switched attenuation input coupling network affected antenna coupler tuning, it must be retained as a termination after the timer is removed).

c. Changes in receiver bandwidth.

d. Replacement of receiver (each receiver has a different internal delay).

2.9.1.2 Local (FPN-54)

a. Change in the FPN-54 sampling point (due to phase modulation); this generally results in an LPA which appears as a time-difference change.

b. Changes in the path between antenna current transformer and FPN-54 input, such as transformer replacement, termination change, etc.

c. Transmitter drive or current sense cable phase reversals and changes in the FPN-54 ETA jump point adjustment (only applicable when used with the new solid-state pulse generator system).

d. Transmitter changes which result in an LPA. Ideally of course, the FPN-54 cycle comp eliminates such need but if the local signal has a large phase modulation component then the remote control-receiver with its different RF bandwidth, will "see" a slightly different phase crossover than the cycle comp and hence the control station will insert an LPA.

Once the receiver is installed and operating properly there should be no need to change parameters and hence there should be no affects from these sources. Station personnel must be aware of what factors can produce changes via the FPN-54 signal so that they are recognized.

2.9.2 Use of a Time-Interval Counter

A time-interval counter measuring between receiver's 1/2 GRR and the FPN-54 1/2 GRR is a most useful instrument in day-to-day receiver operation. If we assume that one time base or the other remains fixed in time (principally the FPN-54 since it is battery backed-up) then slewing and relocking the receiver or slewing the local signal, is simply a matter of slewing until the time-difference returns to the original value. To insure that this relationship does hold, care must be taken not to change either the counter's trigger threshold or PHASE CODE and 0° - 180° switches inside the receiver. Since there is no need to use an oscilloscope to relock the receiver under these conditions there is no need to change any receiver switch settings excepting the slew controls. In the case of a "cold start" after an extended station power failure, the techniques of Section 2.8.3 (using the CYCLE or envelope index information) should be used to first acquire the remote signal, from which the FPN-54 can be resynchronized. Only COCO, Section or District representative should attempt third cycle identification as presented in the Austron Technical Manual. Maintenance of all receiver parameters identical to their setting when this identification was made insures that only the other (counter and "envelope index") techniques need be used to reacquire the Loran-C signal.

2.9.3 CW Interference

Because the receiver does not employ "1/2 GRR" or "FOXTROT" error balancing circuits, it is susceptible to phase errors caused by strong CW interference, even if non-synchronous. Therefore every effort should be made to operate the receiver in an interference free environment. This can usually be accomplished by using the installed Loran-C notch filters at the Loran-C station, which have been optimized over several years for interference removal. The best response to a situation in which a new interfering frequency suddenly appears that obviously causes problems is to shift the receiver to NARROW bandwidth. When this is done and the signal strength is increased (using the receiver's attenuator) by 11 dB, the receiver will track almost as well as in WIDE bandwidth (in a noise sense) and without any degradation in skywave rejection. The latter statement is true simply because the sampling point was not shifted further back into the pulse where there is increased skywave contamination due to the NARROW bandwidth.

The receiver can be operated this way until the interference is removed with an LC notch filter, or disappears. So long as the sampling point is not shifted and any form of lock-on is only performed in WIDE bandwidth, there is only a moderate degradation in receiver tracking performance, seen usually at night as increased fluctuation during higher noise conditions.

2.9.4 Mechanical Construction

The Austron receiver has not been constructed to MILSPEC standards as far as mechanical features are concerned. Field personnel must always consider this and attempt to minimize the number of times the front panel doors are opened and closed and switches are actuated. The following procedures will help insure that this receiver will last for many years in the field:

a. Leave the front panel switch in "Ø" position. All of the other information is readily available on chart recorder display.

b. Leave the SERVO τ switch in the usual nighttime position, there is no need to constantly change bandwidth in a stable cesium/FPN-54 equipped chain.

c. Do not continually readjust the RF attenuator for slight changes in received signal level or differences between remote station's transmitters. The attenuator thumbwheel switches are particularly vulnerable to early failure due to breakdown of the printed circuit foil that forms their internal contacts. Therefore, set the RF attenuator 1-2 dB lower (increasing the signal) that required by the front panel meter set point. This increase in RF signal has appreciable effect on receiver performance but insures that the RF attenuators do not have to be constantly adjusted for remote signal variations.

d. Do not open the front left panel to calibrate the chart recorder once each watch, unless experiments show that major changes have occured within this period. Since the meter can be accurately read to ± 10 ns this provides all of the accuracy required for a DELTA control receiver, even if the recorder calibration changes by 10 percent which is an approximate ± 10 ns variation over a tolerance region centered at the present reading.

2.9.5 Receiver Replacement

Whenever it becomes necessary to replace receivers the time delay through the new receiver should be compared

against the time delay of the old receiver.. The fime delays for wideband operation are stamped inside the receiver on the notch filter cover. If the time delay through the new receiver is less than that through the old, the crisis control number displayed on the time interval counter will increase. The increase will be the difference between delays through the receivers, e.g. Delay new receiver - Delay old receiver = Amount of increase in number. Conversely, the control number will decrease if the delay through the new receiver is greater than the old. Consequently, the receiver should be locked on to the new "control" number. All other connections, settings, etc. should be the same.

2.9.6 FRONT AND REAR PANEL CHANGES

Figures 2-4 and2-5 are the relabeled front and rear panels respectively and should be referred to in lieu of Figure 1-1 in the Austron Instruction Book.

2.10 TWO PULSE LORAN-C TTY COMMUNICATIONS DEMODULATOR

When the W0756-18A/DEMOD Module is incorporated as PCB 12, the Austron Receiver is capable of being used as a demodulator in the Two Pulse Loran-C TTY Communications System. The DEMOD Module is an automatic circuit which tracks a narrowband version of the RF signal being tracked by the receiver (the output of the receiver's "viewing filter"). The DEMOD utilizes timing signals provided by the receiver to process the RF signal and extract the Two Pulse Communications messages.

The DEMOD Module, by itself, is not sufficient to provide a usable representation of the received message. It must be used with a demodulator interface, part of the WO756 Two Pulse Communications Set chassis, to allow interface to a teletype loop.

The DEMOD decides whether or not sufficient modulation is present in the received signal to conclude that a communications message was incorporated in the received signal. The result of this decision is a command to the teletype interface to either do nothing, or send a character on the teletype loop. The DEMOD detects the phase shifts present in the received signal and provides signals to the demodulator interface which indicate what the character to be sent on the teletype loop should be. The DEMOD also decides whether or not a Two Pulse Communications System synchronization signal is present in the received signal. The proper reception of this signal allows the demodulator interface to operate synchronized to the remote transmitter for proper character bit framing.

In making these decisions the DEMOD Module decides where on the received pulses to sample for phase shifts and whether or not to process signals in the presence of atmospheric noise or cross rate interference.

A general description of the Two Pulse Communications System is provided in the System Technical Manual. The specific theory of operation of the DEMOD Module is provided in Section 3.1A of this manual.

3.0 THEORY OF OPERATION

3.1 NINTH PULSE BLINK DETECTOR, PCB 12 (FIGURE 3-1)

3.1.1 Timing Generator

IC timers U6 form the timing generators. U6A is set to approximately 2 milliseconds and times out from the end of the receiver's RF window until a point 60 microseconds after the peak of the ground wave component of the Bandlimited RF input (12C). The latter time is the sampling time to determine if the ninth pulse is present or absent. Q5, R33, and C12 form a bare-collector inverter and delay filter, whose output is coupled back to the timing receiver circuits (8C) to extend the RF window to encompass the ninth pulse. The R33, C12 combination is added to keep the ninth pulse window open past the sampling time to aid the operator in viewing the entire ninth pulse. IC Timer U6B is also started by the end of the receiver's RF window and times out to a point approximately 100 microseconds in front of the ninth pulse. This timing is used to sample the noise-only condition (the equivalent of ninth pulse absent) to set the threshold detector via the CFAR loop.

3.1.2 RF Amplifier and CFAR Loop

IC U1 is a fixed gain RF amplifier, which presents a signal of approximately 2 volts zero to peak to the threshold detector (when the receiver is locked on and tracking at the amplitude set-point). The output of the threshold detector (U2A) is buffered and filtered by Q1, R12, and C4, and Q2. The logic output of Q2's collector represents the decision as to whether each ninth pulse is present or absent. The filter formed by R12 and C4 extends the memory of this decision process over a span of 100 microseconds, resulting in an effective sampling time of 40 microseconds before and 60 microseconds after the peak of the groundwave component of the RF signal input. IC U3B samples, 100 μs before the ninth pulse, the logic waveform from Q2 to form at the output, pin 8, a logic squarewave whose average value represents the number of incorrect decisions (a "one" or signal-present decision was made when it is known that no signal is present before the ninth pulse). U4B filters the squarewave, compares it against the CFAR set-point value formed by R22 and R23, integrates the resulting error and produces at its output the feedback threshold voltage to the threshold detector U2A. Thus, when the noise level rises, an increasing number of incorrect

or logic "one" decisions will be made, which will bias the input of U4B resulting in the accumulation of charge on C5 and an increasingly negative threshold voltage applies to pin 4 of U2A. This effectively raises the threshold with respect to the noise (in a negative direction, but a rise in an absolute sense) and reestablishes the null condition of this Type I servo loop.

3.1.3 Frame Synchronization Circuit (Figure 3-1 and 3-2)

The output of U3A represents the sampled decision as to whether the ninth pulse is present or absent. This is processed by U4A, U2B, U10, and U9 to form a timing window which straddles the "dot" identifier code of the local station, when the master's ninth pulse is blinking. For this reason, it is termed a frame synchronization circuit in that it synchronizes the local station code sampling pulse to the frame or basic 12 second period of the master's blink code. See Figure 3-2 for a time ladder diagram. U4A, a non-symmetrical integrator, sums a number of "one" decisions as seen at the output of U3A. When at least nine tenths of a second of consecutive "one" decisions have been summed by U4A, the output passes a negative threshold as sensed by U2B. U2B's output transition then marks approximately the end of the "dash" portion of the master's blink code (this dash occurs from time 0.5 to time 1.5 seconds within the basic 12 second master blink cycle). IC timer U10B times out from the end of the master's "dash" to the time of occurrence of the local

station's dot code. At the same time, U10A times from the same starting point as U10B for 10 seconds and inhibits further transitions of U10B. This then forms a one-step phase-lock to the known 12 second period of the Master's blink code. U9A times from the end of U10B's time-out for a period of 0.5 seconds to actually sample the ninth pulse "one-zero" decisions during this period, and to determine on an average basis if the local station is being blinked. The resistor timers of U10B must be factory chosen for the actual value of C18, the timing capacitor of that unit. The timing for the X-ray secondary, which has only one "dot" in its code, is the most critical, whereas the least critical is Whiskey.

3.1.4 Sampling and Detection Circuitry

The sequence of master ninth pulse decisions, when the master is transmitting the basic blink code, is sampled during the local station's "dot" by FET Q7 and averaged by R45 and C17. This averaged signal is buffered by U8, further filtered by R37 and C15, buffered by Q6 and finally compared against the decision threshold set by R36 and R35 by U7B. The output of U7B, when the sample voltage at pin 10 exceeds the threshold, goes low which turns on the front panel blink LED (6C) and actuates the logic low to the rear panel connector (5C). R36 provides hysteresis in this decision

threshold, such that once the decision is made, the input voltage must change by greater than 0.5 volts before U7B "decides" the blink has been turned off. The choice of the threshold voltage for U7B is a complex one, based on the peak-to-peak fluctuations of the voltage at the emitter of Q6 seen when the master is not blinking and when the master is blinking another station. This voltage is a random process, since all circuits in the system will be from time to time erroneously tripped by noise. The decision voltage at U7B must be chosen to reduce erroneous or blink false alarms (another station is being blinked) to a very low level, while at the same time, being low enough such that local station blink will be detected within a reasonable time period.

CR3, CR4, and U5 form a threshold detector for the output of the U4A integrator. When the master ninth pulse is not blinking, the signal at U1 is there essentially continuously resulting in a constant logic true level at the output of U3A. This drives U4A to negative saturation, approximately -11 volts. At -10 volts, the diode threshold detector changes state and the inverted outputs of U5A and U5B are applied to the memory capacitors C15 and C17 to clear these capacitors. This circuit, in conjunction with the pseudo-phase lock timer U10A prevent false blink detection when the Master is not blinking any station.

The blink detector circuit is a sophisticated system whose performance depends upon a number of design parameters. Most of these parameters, such as the CFAR loop set point (the percentage

of incorrect decisions), the detection threshold and the bidirectional integrator slew rates were selected after a careful statistical analysis and laboratory tests. They should NOT be changes since they all interact, and together set the two observable characteristics of the detector; time-to-detect-blink, and false alarm rate. The former can be easily measured when the remote signal SNR is high by the test blink procedure of 3.1.5 below. The causes of the latter are not obvious, but fall into two categories:

False Alarm, Blinking. This alarm occurs when the master is blinking another station and the local detector alarms. When the CFAR loop output voltage is more negative than -0.4 volts the loop is active and this type of false alarm occurs at a fixed rate of about once per five hours of blink-time, irrespective of further increases in noise level. This rate varies in a negative exponential fashion with the value of R45 (a field variable component) and hence can be easily decreased if one is willing to accept a longer time-to-detect-blink. When the CFAR voltage is clamped at -0.4 volts, the noise is insignificant and the CFAR loop is essentially disabled, whence this false alarm rate becomes zero.

False Alarm, Non-Blinking. This alarm occurs when the frame synchronizing circuit begins to frame randomly on the noise pattern of ones and zeroes. This is the highest noise level (or lowest SNR) at which the blink detector can operate. The onset of this condition is very abrupt. As the noise increases by 1-2 dB, or SNR decrease (e.g., due to skywave cancellation of the groundwave), this alarm rate changes from zero to 1-2 alarms per-minute. An accurate determination of when this point has been reached can be made by averaging (with an RC filter of about 100 kΩ and 100 μF) the logic waveform at TP2. This waveform is the record of one-zero decisions made at the ninth pulse time. When this average voltage decreases below about 3.5 volts (the number of ones is less than 2.5 times the number of zeroes) the bidirectional integrator becomes hopelessly confused and crosses and recrosses the -5 volt threshold, repeatedly tripping the timing and sampling circuitry. The onset of this alarm condition is very nearly the fundamental limit of any envelope type code detector system. Attempts to extend this limit 1-2 dB further result in major degradations to time-to-detect blink under normal conditions.

3.1.5 Test Blink Circuit

The blink waveform from the standby TD989 is injected at TP6; this waveform, less the first "dit", is a replica of the master ninth pulse blink code. When this waveform is low the FET Q9 switches in C26 which increases the "on" time

of U6A. With the increased timing U1 and U2A sample beyond the ninth pulse where there is only noise, but no signal. U3A output thus goes low; but when Q9 switches off and restores the original timing U3A goes high because the ninth pulse is in fact present. In this fashion U3A replicates the local station master blink code when in fact it is not being transmitted. The rest of the circuits perform their normal function so that one or so minutes after starting "test blink" the BLINK ALARM goes off.

3.1.6 Power Supplies

The ninth pulse blink detector uses the +5 volt logic supply of the Austron timing receiver and has an on-card DC to DC converter to generate ± 15 volts from the unregulated 20 volt Austron receiver supply.

3.2 RF INPUT PROTECTION (REFER TO FIGURE 3-3)

Back to back silicon diodes (1N914) are connected between the junction of R61 and R58 and the base of Q1 and the R60 junction. This location effectively puts the diodes across the input transformer on the amplifier side of the

input resistors. These resistors then provide current limiting and power dissipation such that the diodes themselves are not damaged by large antenna input signals.

3.3 CROSS RATE BLANKING (REFER TO FIGURE 3-11)

Cross rate blanking is brought into the receiver via a rear panel jack, J-22, and connected to J7-7C thru a 1N277 diode. A 470 Ω resistor is connected between 7C and IC73-Pin 6 on PCB 7 to provide a load across which the RF Window B waveform can be dropped during periods of cross rate blanking. In addition a jumper is connected from Pin 7 of PCB 7 to IC81-Pin 9. The net result of these changes is to blank the RF Window B and Phase Code B waveforms during the period of the cross rate blanking waveform.

3.4 1-2 GRR OUTPUT (REFER TO FIGURE 3-4)

An unused D FLIP FLOP on the GRP divider is used to reclock the approximate 1/2 GRR waveform available within the receiver to the precise timing of the phase strobes. The phase gate generated by the GRR divider is applied to the clock input of IC 91A, and the D input is brought over as GRP from PCB-7. Thus, the state of the GRP waveform is "read" by the phase gate and hence the output 1/2 GRR waveform is retimed to the phase gate timing.

3.5 START-STOP PHASE COMPARATOR (REFER TO FIGURE 3-5)

IC41 and IC43, which provided 10 kHz and 100 kHz to the original 10 and 100 µs phase comparators, have been removed. In their place, mounted on a sub board attached to PCB 9, has been installed a retriggerable one shot multivibrator IC31 and quad two input nand gate IC41.

This modification changes the phase comparator to 1 µs operation. The output of the phase comparator is used as drive for a strip circuit. The circuit has provisions for recorder pen centering and terminal jumpers are provided to achieve crossover range flexibility.

The circuit compares a reference 1 MHz to the receivers phase shifted 1 MHz. The difference in phase produces a duty cycle change in the output waveform, as the duty cycle changes the average voltage available for the recorder pen drive changes. i.e., As TD changes, the duty cycle changes and the average recorder voltage changes.

An unused D FLIP FLOP on the GRO divider is used to reclock the approximate 1/2 GRR waveform available within the receiver to the precise timing of the phase strobes. The phase gate generated by the GRR divider is applied to the clock input of IC 91A, and the D input is brought over as GRP from PCB-7. Thus, the state of the GRP waveform is "read" by the phase gate and hence the output 1/2 GRR waveform is retimed to the phase gate timing.

3.5 START-STOP PHASE COMPARATOR (REFER TO FIGURE 3-5)

IC numbers 41 and 31, which provided 100 kHz and 10 kHz to the original 10 and 100 microseconds phase comparators, have been removed. In their place, have been installed a retriggerable 1 shoot multivibrator (IC number 31) and a quad two input nand gate (IC NUMBER 41). The phase comparison is still performed by IC 21A exactly as described in the Austron Technical Manual. The output of this flip flop (21A) besides going to the phase averager and output driver is coupled to the input of the retriggerable one shot (IC31). So long as transitions occur at the output of the phase comparator flip flop, the one shot is retriggered and its output stage remains at the logic true state. When the output of the phase comparison flip flop no longer exhibits transitions (meaning that the start-stop timing relationships have entered a deadband) then the retriggerable one shot times out and the output changes state, which causes flip flop 21B to toggle and connects the inverted phase of the start waveform to the input of flip flop 21A phase comparator. This selection of a phase inverted signal immediately restarts the phase comparison flip flop and again latches up the retriggerable one shot and of course adds 0.5 microsecond shift to the phase comparator output. The definition of which line is start and stop is explained by Figure 2-2.

A spare inverter, 1/4 of IC number 43 is used to buffer the output of the 1 MHz signal from the voltage controlled oscillator to provide the frequency standard squarewave at the rear panel. This 1 MHz signal, because it is taken at the output of the voltage control oscillator, will exhibit short term fluctuations of approximately 0.1 microsecond peak-to-peak, referred to the input 1 MHz from the frequency standard.

The start input (reference 1 MHz) drives the retriggerable one shot multivibrator IC31 where its duty cycle is changed by the mid-scale adjustment to allow the recorder pen to be centered. The reshaped reference 1 MHz is inverted by IC41D as they start waveform for flip flop IC41A/IC41B. The stop input (phase shifted 1 MHz) is fed via a range circuit consisting of inverter IC41C and range jumpers 3, 5, 6, to IC41A/IC41B as the stop waveform. The range circuit is used to select the duty cycle range that will allow the mid-scale adjustment to have centering capabilities of approximately 2-7 μs and 7-2 μs.

3.6 RECEIVER RF GAIN (REFER TO FIGURE 3-6)

The effective RF gain of the receiver as seen by the phase tracking loop is increased +12 dB by attenuating the RF signal seen by the amplitude sampling circuits -12 dB. Thus, to achieve the proper amplitude set point, the RF gain is increased via the input RF attenuator until the amplitude set point is reached which results in a net +12 dB gain of the RF signal tracked by the phase lock loop on PCB 2. Figure 3-6 shows among various other changes in the output wiring the two resistors, 330 Ω and 100 Ω, that achieve this effective 12 dB increase.

3.7 NOISE LIMITER (REFER TO FIGURE 3-7)

The noise limiter is inserted in series in the phase strobe sampling circuit. The RF signal is AC coupled and

referred to the +10 volt analog ground by C3. The signal is then amplified 20 dB by the operational amplifier type NE531. This amplification establishes the noise clipping point with respect to the volt per microsecond transfer curve of the phase strobe sampling network. The series 1 kΩ resistor and matched germanium 1N277 diodes form the actual noise limiter. Due to the series resistor, this limiting is not a sharp clipping action, but rather a somewhat soft logarithmic type limiting once the signal at the output of the NE531 reaches approximately 300 mV. The following two resistors form a 20 dB attenuator, whose output impedance exactly equals the 2.2 kΩ source resistance originally seen by the Austron sampling network, consisting of Q1, and Q2. Thus, when the SNR is large, the receiver acts exactly as designed by Austron in terms of the transient response of the phase tracking servo. When the SNR (as measured at the sampling point) decreases below about +3 dB, the noise limiter begins to take effect and limits voltage excursions which, on a single sample basis, represent an error greater than approximately 2-1/2 μs. The net effect of such non-linear action is to ultimately reduce the phase tracking loop bandwidth, due to the effective suppression of the RF signal by the limited noise. Thus, the receiver exhibits the well known characteristic of hard limited receivers in that it tends to be self-adaptive to increasing noise levels. It reduces the phase tracking loop bandwidth as the noise increases.

3.8 SIGNAL AND AMPLITUDE RECORDER OUTPUTS (REFER TO FIGURES 3-8 and 3-9)

Figures 3-8 and 3-9 show the two-transistor DC amplifier which has been added to both PCB 3 and 4 to subtract a DC voltage from the normal signal and amplitude outputs and amplify the resulting DC component plus AC signal component by a factor of 2. The 1 kΩ potentiometer provides the subtraction voltage to the emitter of the NPN transistor where it is differenced with the output of the SIGNAL and AMPLITUDE DC amplifiers. The following PNP stage acts as a +6 dB DC coupled gain stage and a level shifter to return the output signal to chassis ground for use by voltage type recorders. The output impedance of this circuit is 10 kΩ and hence it should only be connected to a voltage recorder of at least 100 kΩ or greater input impedance. The 1 kΩ potentiometer is factory adjusted to provide a signal which in the case of the SIGNAL output deflects from approximately 1/4 to 3/4 full scale at the sampling point, as seen on a Brush type voltage recorder, and in the case of the AMPLITUDE output, results in a normal amplitude sampling value of approximately 40% full-scale on a Brush recorder. The adjustment of this potentiometer, coupled with the adjustment of recorder gain, can provide any ratio desired of the slowly varying AC component of the SIGNAL and AMPLITUDE outputs relative to the DC or offset component. Thus, for example, one could readjust this resistor so that the entire

pulse can be displayed on a recorder without distortion with an accompanying reduction, of course, in the amplitude at the sampling point. The factory adjustment is recommended for easist identification of the correct third cycle sampling point crossover.

3.9 TWO PULSE COMMUNICATIONS SYSTEM DEMODULATOR (PCB 12, FIGURE 3-12)

3.9.1 DIGITAL TIMING GENERATOR

3.9.1.1 Track Strobe Generator.

Receiver track strobes (RSTR-L) which are locked to the normal tracking point of the Austron 2000C, are applied to U7 and U14. U7 counts the track strobes during each RF Window period and allows one-shot U14 to fire twice per GRI: during pulses 7 and 8 if U7-10 is jumpered to U7-11; during pulses 1 and 2 if U7-10 is open. While U14 is timing out, it holds counter U27 in a reset (state zero) condition. Once the timeout of U14 is completed, U27 is allowed to count the receiver 100 kHz positive going transitions. U28 decodes the states of U27: it indicates state zero while U14 is timing out, state 1 for 10 µs beginning with the first positive going transition of the 100 kHz after U14 has timed out, state 2 for the next 10 µs, etc.

While U27 is in state 1, U28 provides an initializing pulse to the Analog Signal Processing Section (C-ASP-1). The 10 μs period decoded by U28 as state 2 is designated the Groundwave Sampling Strobe (GWSS). The 10 μs period decoded as state 8 is designated the Skywave Sampling Strobe (SWSS). When state 9 is decoded, U28 forces U27 to assume state 9 after all succeeding 100 kHz positive going transitions until a reset pulse is applied (by one-shot U14).

In summary, the track strobe generator section provides three 10 μs strobes twice per GRI. The location of these strobes in relation to the receiver track strobes can be adjusted by trimming R12 which controls the timeout of U14. The timeout is adjusted, upon installation of the WO756-18A/DEMOD Module, so that the groundwave strobe is located at the peak of the narrowband RF signal if there are no skywaves present in the received signal. This is illustrated in the Time Ladder Diagram of Figure 3-13.

3.9.1.2 Phase Locked Loops and Loop Signal Multiplexer

The phase locked loops utilize the receiver 10 MHz clock to synthesize waveforms locked to certain zero crossings of the hardlimited narrowband received RF signal provided by the Analog Signal Processing Section. C-PLL-1 tracks

the positive to negative transition of the hardlimited RF signal occurring with the 10 μs time limit of the groundwave sampling strobe (GWSS). C-PLL-2 tracks the transition occurring within the 10 μs SWSS. A logic signal provided by the Analog Signal Processing Section, to be described in a later section, commands the loop signal multiplexer to choose its output signal to correspond to the signals provided by one or the other of the two phase locked loops. Except for the fact that they process the hardlimited RF signal during two different 10 μs intervals, the operation of C-PLL-1 and C-PLL-2 are identical. Consequently the description provided will be based on the situation in which the loop signal multiplexer is being commanded to route signals from C-PLL-1 to its output. Similar waveforms (perhaps offset slightly in time) are being generated by C-PLL-2 but are simply not being selected for use by C-LSM-1.

U1 and U4 form a modulo 100 counter which defines the states labelled in the timing diagram of Figure 3-14 by counting the Austron Receiver's 10MHz signal (the counter chain normally counts from state 00 to state 99). The signals shown in Figure 3-14 are present throughout the group repetition interval and, presuming no phase shifts are ordered, are periodic - occurring every 10us (100 counts of 10 MHz). Twice per GRI (during the GWSS 10us

periods which occur during pulses 1 and 2 or 7 and 8) the phase sensitive detector part of the loop is enabled. This portion consists of cascaded up/down counters U2 and U3 (for C-PLL-1, U10 and U11 for C-PLL-2). U2 and U3 can define 256 unique states - changing state only on the same 10 MHz waveform transition that causes the modulo 100 counter chain to go from state 99 to its next state and located within the GWSS 10 μs duration. The up/down counters count up if the delayed hardlimited RF signal is in the high state at the time of this clock transition, down otherwise. Depending upon the amount of noise in the received signal and the time difference between the high to low transition of the hardlimited RF and the PLL 100 kHz signal (count 99 of the modulo 100 counter), the up/down counter chain will eventually overflow or underflow. If the counter overflows - caused by a predominance of clock pulses (occurring at the trailing edge of the PLL 100 kHz) when the hardlimited RF waveform was in the high state - it is presumed that the PLL 100 kHz waveform is occurring too early in time - as defined by the hardlimited RF signal (refer to Figure 3-14). It would then be desirable to delay the PLL 100 kHz signal. This is accomplished by making the modulo 100 counter, upon overflow of the up/down counter, count one additional clock pulse for one 10 μs period (the counter goes from state 99 to state 99 to state 00 to state 01, etc.). The PLL 100 kHz waveform is thereafter delayed one counter of 10 MHz - 100 ns - and is presumably closer to being aligned with the high to low transition of the delayed hardlimited RF signal.

If the count

If the counter underflows - caused by a predominance of clock pulses when the hardlimited RF is in the low state - it is presumed that the PLL 100 kHz waveform is occurring too late in time. Upon underflow, therefore, the modulo 100 counter chain is made to skip one count for one cycle (it counts from 99 to 01 to 02 etc.) so aht the PLL 100 kHz waveform is advanced 100 ns in time. In case of either overflow or underflow, the up/down counter is reset to a midrange value of 128.

2.9.2 Analog Signal Processor

Note: Potentiometer R11 is used to position voltage level "Analog Reference" (AR) at a value approximately 200 mV above the +10 V buss. The receiver narrowband RF signal is AC-coupled into the WO756-18A/DEMOD Module and biased at the AR level.

3.9.2.1 Signal Limiter and Detector

Voltage comparator U16 is used to hard-limit the incoming narrowband RF signal. R34, C11 and the second comparator of U16 are used to delay the hardlimited signal approximately 300 ns. R49, R50, CR8, C15, and U26 are used to produce a trigger, approximately 200 ns in duration, at the high to low transition of the non-delayed hardlimited RF signal. The output waveforms from this section are as shown in Figure 3-15. It is the delayed hardlimited RF signal that the phase locked loops lock on to.

3.9.2.2 Amplitude Tracking Loops

Except for the fact that they are enabled at different times, the two amplitude tracking loops are identical in operation. Consequently, the operation of C-ATL-1 only will be considered.

A voltage level representative of the minimum value attained during the GWSS of the combined signal - analog reference plus narrowband RF - is applied to Pin 5 of voltage comparator U17. The two inputs to this section of U17 are illustrated in Figure 3-16.

The purpose of the loop is to maintain the level at U17-5 at a point where it matches the minimum value of the RF as shown. If the incoming RF signal increases slightly in magnitude it will cause a pulse (or pulses) to appear on U17-2, the output of the voltage comparator. If a pulse occurs during the GWSS 10 μs time period, it will reset flip-flop U18 U18-14 will then go to a 5 V level. This voltage level, being greater than the 2.5 V applied to U19-3, will cause C8 to slowly discharge through R28.

This brings the level at U17-5 down. This level will continue to slowly decrease until just before the next GWSS when the loop initialization pulse (10 μs in duration - state 1 of U27) sets flip-flop U18, forcing U18-14 low. If the voltage level on U17-5 has not decreased enough so that it is at or below the minimum value of the signal on U17-4 during the GWSS, another pulse will be produced at U17-2, resetting U18 and forcing U18-14 high again. The capacitor, C8, will continue to slowly discharge.

Eventually, the level at U17-5 will decrease to a point at which it is below the minimum value of the RF signal at U17-4. At this point, U18 will be set by the initialization pulse and remain set since no clock pulse will be received from U17-2 during the GWSS. With U18 set, U18-14 is low - a level below 2.5 V. This causes C8 to slowly charge up - thereby increasing the signal level at U17-5. In this fashion, the level at U17-5 can move up or down in response to changes in the amplitude level of the narrowband RF signal within the GWSS. It therefore represents a long term average of the GWSS RF signal level.

Notice what occurs if the RF input is removed. The level at U17-5 will continually rise in search of the RF signal which will, by passing below and then above its level, cause a pulse on U17-2 which will check the rise of the voltage at U17-5. If

this voltage rises too high, it will achieve a level high enough so that when the RF is returned, it is unable to "recapture" the long term average signal (since the RF is always below this level, it can not pass below and then above). This problem is overcome by use of CR4 which clamps the long term average germanium diode drop above the +10 V buss (at about 10.3 V). For this reason, we set AR at about 10.2 V (more precisely, .2 V above the +10 V buss) and insure that we have, normally, at least 100 mV o-p of RF signal (600 - 800 mV p-p is a good level to set it at to insure this).

3.9.2.3 Track Point Selector

The long term averages of the GWSS and SWSS signal amplitudes are compared (with a small amount of hysteresis) by U19. U19-8 is low if the GWSS has a larger signal amplitude, high if the SWSS does (Note that if the GWSS has a lower signal amplitude than the SWSS U19-10 will be lower than U19-9). In U15, this signal gates through one of the two sampling strobes (the one with the larger amplitude) to become the Real Time Strobe. U15 also allows the use of a signal which can inhibit data processing. This signal is developed in the Samppling Decision Network and will be described later.

The signal from U19-8 is used by the Loop Signal Multiplexer so that signals from the loop corresponding to the sampling strobe with the greater signal amplitude can be selected. U19-8 also controls FET Q1 which, in conjunction with isolation resistor R26 approximates a SPDT analog switch. This switch routes the selected long term average amplitude (the larger one) to the Sampling Decision Network.

3.9.2.4 Sampling Decision Network

The selected long term average is applied to U17-10 where it is compared to an attenuated version of the narrowband RF (i.e., the peak is moved closer to AR). If the attenuated RF signal nevertheless drops below the selected long term average, it fires a retriggerable one-shot, U20. This one-shot being fired implies that even an attenuated version of the RF is greater than the average amplitude so that it can be presumed that some sort of contamination - cross rate or atmospheric noise must be present.

The selected long term average is attenuated and applied to U17-8 where it is compared to an unattenuated version of the RF. The result of this comparison should cause the one-shot to fire. If the one shot does not fire, it is presumed that, since the RF has such low amplitude, it is contaminated or absent due to remote cross rate blanking.

One-shot U14 is used to extend the cross rate blanking waveform. The presence of this extended blanking waveform resets both one-shots of U20.

The only valid state during which it is desirable to process the incoming pulse for communications data occurs when U26-2 is low and U26-1 is high. Notice that this is the only possible state which will cause U26-3 to be high. If U26-1 is low it means that the RF was less than the attenuated long term average. Clearly, the attenuated RF must be lower than the unattenuated long term average so that U26-2 can not be high. Whenever U26-3 is low the Real Time Strobe is blanked. This inhibits any data processing.

3.9.3 Digital Signal Processor

Figure 3-14 is repeated as Figure 3-17. The Real Time Strobe is present during the 10 μs duration of the sampling strobe during which the greater RF signal amplitude occurs and when the Sampling Decision Network has not ordered that sampling be inhibited. It is only during the Real Time Strobe that any of the three subsections of the Digital Signal Processor are enabled.

3.9.3.1 Communications Modulation Detector

U25 combines the Real Time Strobe, counts 94-99 of the selected Phase Locked Loop, and the RF Transition signal (U26-8). The leading edge of the RF transition normally occurs at about count 97 of the PLL and is approximately 200 ns in duration. Consequently, there will be a pulse of sufficient duration to trigger U23 as long as the RF Transition is within about 300 ns of its average reception time. Counter U23 is given an entire character period to reach its programmed terminal count: 8 or 15. If the terminal count is reached, the counter is latched up and a modulation <u>not</u> present signal is produced. The character delimit signal is received from the demodulator interface (external to the Austron receiver) at the beginning of each character period.

In view of the fact that a fixed number must be programmed as ther terminal count while a variable number (anywhere from 0 to 4 MN where M=# of bits per character and N=# of PCI per bit) of pulses may be processed per character period, it can be seen that this method of detecting modulation is suboptimum. This method is necessitated by lack of space on the WO756-18A/DEMOD Module and represents a carefully designed open loop solution to the modulation detection problem. Experience has shown that the terminal count should be programmed at 8 unless MN is greater than about 10.

3.9.3.2 SYNC Bit Detector

U15 selects as its output counts 70-79 of the PLL during GRI A and counts 20-29 of the PLL during GRI B. From Figure 3-17 it can be seen that when a SYNC bit is transmitted (the signal is advanced 2.4 μs during GRI A and retarded 2.4 μs during GRI B), the RF Transition waveform will move from its normal location - lined up with count 97 of the PLL - to occur at count 73 during GRI A and 21 during GRI B.

High Pass Filter C3-R6 shortens the two 1 μs SYNC windows so that they are, effectively, counts 70-74 and counts 20-24. This decreases the chance of a SYNC bit false alarm. The RF transition is gated with these windows at U8 and is applied to the clock input of U29. U29 is asynchronously preset to state 4 at the beginning of each PCI. If all four pulses representing the SYNC bit are received in the proper SYNC detection windown, U29 Q_D will go high indicating the detection of a SYNC bit in the received signal.

3.9.3.2 Bit Phase Detector

Two exclusive OR gates utilize the PCI waveform (high during GRI A) and the signal from U7-5 (high during even numbered pulses of a GRI) to decode the hardlimited RF. If a 1-bit were transmitted, the 4 communications pulses would be decoded to appear as in Figure 3-18(a) (assuming no noise in the received signal). If a 0-bit were sent, the decoded waveforms would be as in Figure 3-18(b).

If the decoded RF waveform is high at the time of the leading edge of the PLL-100 kHz waveform, a pulse is produced on pinout 19C. If it is low, the pulse appears on pinout 20C. These two signals are used by the demodulator interface to form the detected bits of each character.

4.0 MAINTENANCE AND TROUBLESHOOTING

The Austron 2000C Timing Receiver is not designed for field troubleshooting, repair and calibration. In the event of any apparent malfunction of the receiver, such fact should be immediately reported, in accordance with current directives. The maintenance and especially the calibration procedures described in the Austron Technical Manual should not be attempted by field personnel, since they are only necessary in the event that discrete components on the various printed circuit modules are replaced. The modifications described in this Addendum to the the technical manual do not in any way affect the Austron alignment and calibration instructions. However, when the calibration procedures are executed by a second line maintenance facility, the calibration of the signal and amplitude offset buffers (described in Section 3.8 above) must be rechecked.

4.1 CHASSIS CHANGES TO MODIFY AUSTRON 2000C-1 TO A 2000C-2 RECEIVER

A new green binding post, jack E-16, has been added to the rear panel. It is labelled CALL and is internally connected to PCB12-18F. The Blink Alarm, jack E-15, has been relabelled to CODE and is internally connected to PCB12-5C.

4.2 OPERATING INSTRUCTIONS AND HOOKUP FOR AUSTRON 2000C-2 RECEIVER NINTH-PULSE COMMUNICATION PROVISION

The output of the Communication Blink card is available as a audio frequency signal at the rear panel binding posts labelled "CALL" and "CODE". The user should provide a SPDT switch and a 4 ohm speaker to connect to these outputs and ground, as shown in Figure 4-1

It is intended that the "CALL" output be monitored until the warbling signal is heard and then the speaker switched to the "CODE" output for the message. Upon the termination of the message, the speaker should be reconnected for the "CALL" function.