Massachusetts Institute of Technology

CO

W-234 TIMING LOR-C

Cours

Used

19

Massachusetts Institute of Technology

COMPUTATION BOOK

NAME	Nu
William A. Cooper, ETC	258- 7

W-23

Cours AN/FPN-41

Used om 14 March 1961, to

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

COMPUTATION BOOK

GENERAL INSTRUCTIONS

In all work in which *accuracy* and *ease of reference* are important, much depends upon carrying out the computation in a systematic manner. The following instructions, taken from the *Engineering Department Figuring Book of the Allis-Chalmers Co., serve as a guide in this matter.*

"All computations, of whatever kind, are to be made in these books, except in cases where special blanks may be provided for specific kinds of computation. Computations may be made in ink or pencil, whichever may be more convenient. Pencil figuring should be done with a soft pencil. All the work of computation should be done in these books, including all detail figuring."

"Each subject should begin on a new page, no matter how much space may be left on the previous page. The subject, with the date of beginning it, should be plainly written at the top of the first page of the subject."

"Work should be done systematically, and as neatly as consistent with rapidity. The books are, however, intended for convenience, and no unnecessary work should be done for sake of appearance only. Errors should be crossed off instead of erased, except where the latter will facilitate the work. Work should not be crowded. Paper costs less than the time which would be expended in attempting to economize space in making erasures."

"Where curves drawn on section paper (or sketches) are necessary parts of a computation, they should be pasted in the book, except where specifically otherwise provided for."

"Computations should be indexed, in the back of the book, by the person using the book."
* * * * * * * "

TECHNOLOGY STORE
HARVARD COOPERATIVE SOCIETY, Inc.
40 Massachusetts Ave., Cambridge 39, Massachusetts

Hewlett Packard - Time Comparator
Model - 114BR.

1-1. The comparator is used in making comparisons against the 1 second timing pulses (ticks) transmitted from WWV, (WWVH) or similar source of master pulse.

1-2. The instrument permits the addition of a controlled delay to the 1pps local clock tick from the time standard system, provides a simple means of measuring the time difference between the 1pps local clock ticks and master (WWV, etc) without requiring phase adj of 1 pps clock ticks.

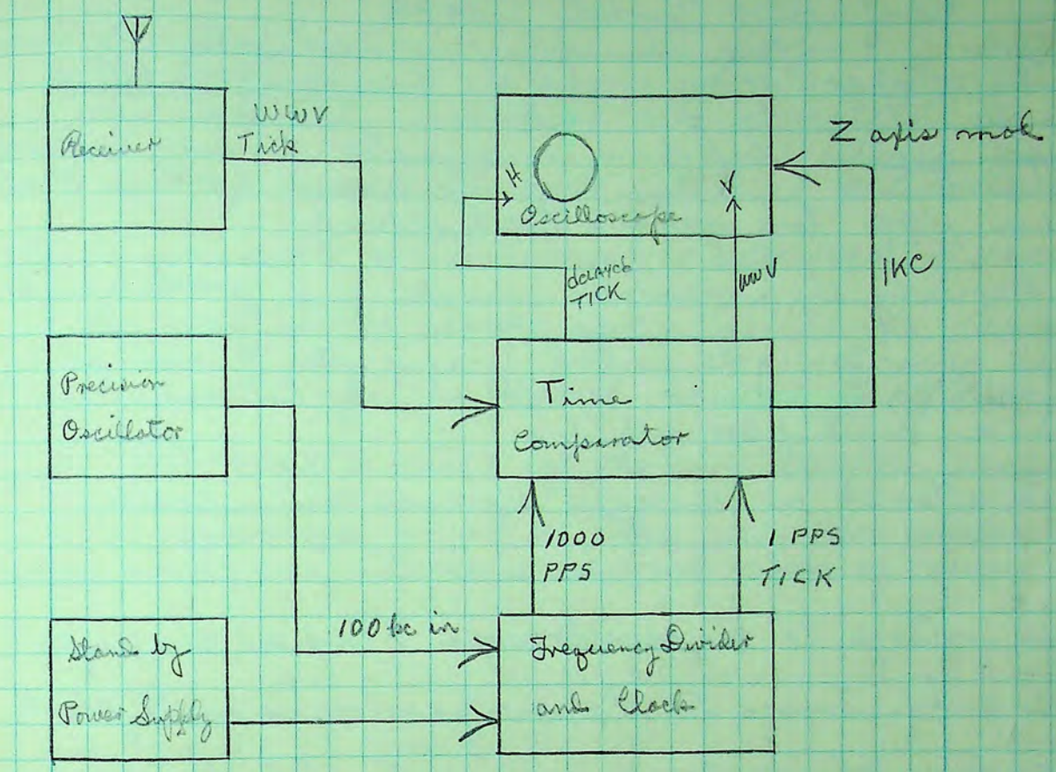
1-3 The 1 second timing pulses (Ticks) as transmitted by WWV normally consists of a 5 milli second, 1000 cps sine wave (WWVH, 1200 cps), with exact time represented by the leading edge of the pulse. This signal is displayed on the scope using a sweep generated in the comparator (continued → P. 2) over

1-4 Comparator 114BR (cont)

The comparator introduces time delays in multiples of 1 millisecond up to 1000 milli. The 4 sweep times available are 1000, 100, 10 and 1 millisecond. Any one cycle of WWV may be displayed on the screen when using the fastest sweep (1MS). Ten intensity markers are displayed on all sweeps to aid in time calibration. On the fastest sweep (1MS) range the markers occur at 100μs intervals and the WWV waveforms are modulated by a synchronized 50kc square with produces a dashed trace with each dash and space equal to 10μs. The time interval between the clock ticks and a selected reference point on the WWV tick can therefore be obtained to the nearest millisecond from the comparator front panel settings and to the nearest 10μs from the oscillator interpolation.

1.5. The comparator is normally used in a system concept consisting of a precision oscillator, a clock frequency divider, a clock and an oscilloscope, such as in Drawing 1-5a.

Figure 1-5a.



1-6 The clock keeps correct time indefinitely, if the precision oscillator driving it maintains its exact nominal value. With the comparator in the system, fast and accurate time checks can be made daily. Time error is recorded in a system log and serves as a correction figure to bring the clock tick into coincidence, or near coincidence with the WWV tick. The data thus accumulated over a period of weeks and months may be used to determine the long drift of the precision oscillator.

1-7 Basic operation (Hewlett Packard)
Comparator Model 114BR

The comparator measures the time interval between a 1 pps master tick from a master timing source and a 1 pps tick from a local clock.

Basically, the comparator consists of a preset counter, sweep generator, gate control, Y-axis gate, Z-axis gate and a multiplier circuit.

An external oscilloscope serves as an indicator.

The sweep generator provides a continuous sweep saw tooth voltage to the oscilloscope X-axis. An input 1 kc pulse train to the comparator is multiplied to 50 kc; the 50 kc signal, controlled by the Z-axis gate, serves as the oscilloscope unblanking signal.

The Y-axis gate controls the application of the master tick to oscilloscope vertical axis.

The local clock tick is delayed by the preset counter, whose output triggers the gate control at a 1 pps rate. When Y- and Z-axis gates are opened by the gate control the sweep is unblanked, thus allowing presentation of the master tick. By adjusting the

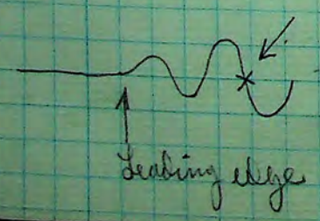
time delay and sweep speed, the master tick can be displayed in expanded form.

Ten intensity markers are available on each sweep speed to aid in time calibration. The time interval between the occurrence of the master and local ticks is equal to the delay time inserted by the preset counter plus the time between the start of the oscilloscope sweep and a reference point on the master tick.

SYSTEM LOG

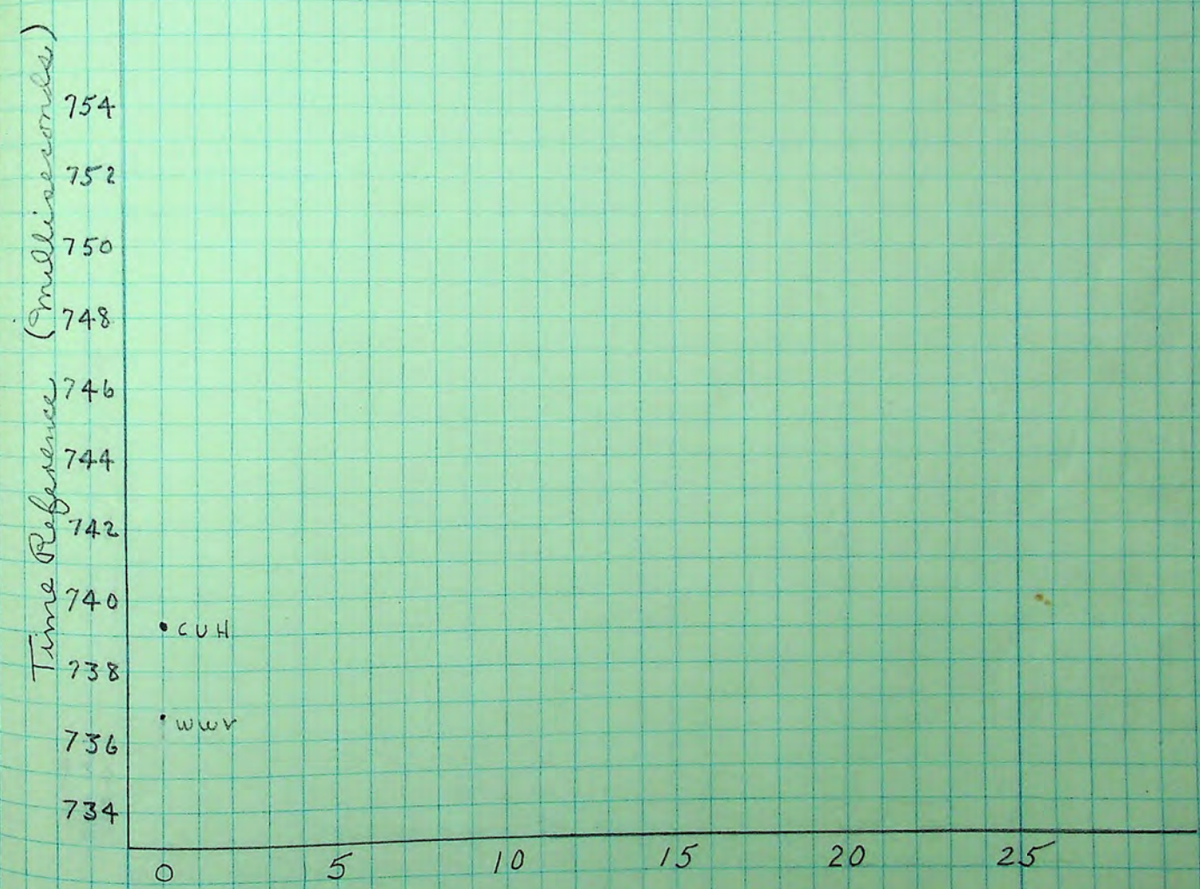
DATE	TIME	SUPPLY: BATTERY VOLTAGE BATT	SUPPLY: BATTERY VOLTAGE LOAD	SUPPLY: BATTERY CURRENT BATT	SUPPLY: BATTERY CURRENT LOAD	BATT CHK	OSCILLATOR: OUTPUT E	OSCILLATOR: OUT I	OSC OUT	IP 1	IP 2	IP 3	IP 4	IP 5	10 6	10 10	CIRCUIT CHECK: SUPP	100 KC	10 KC	1 KC	CLK CURRENT	TIME REFERENCE: MILLI-SEC	TIME REFERENCE: MICRO SEC	RADIO RECP COND
2/26	1345	28			90ma		135	39	60	80	105	101	95	100	20	17	6.2	8.3	6.5	6.8	6.7	736	593	Fair

REMARKS: Measurements made at zero crossing of the second cycle at center vertical graticule of scope.



$\frac{\Delta f}{f}$ = average frequency error.

$$\frac{\Delta f}{f} = \frac{(t_2 - t_1)}{\text{Day}} \times \frac{1\ \text{Day}}{8.64 \times 10^{10}\ \mu s}$$



Readings made at 1406 WWV and 1405 CUH

Time Comparison Chart

		WWV		CUH	
Month Day		Time Reference		Time Reference	
		M sec	μ sec	M sec	μ sec
Feb 26	0	736	593	739	346
27	1				
28	2				
29	3				
M 1	4				

PROJECT W-234 : LORAN-C STANDARD TIME TRANSMISSION

"PROJECT REQUIREMENTS"

① AN/FPN-41 & FPN-42 equipment.

(a) Provide a 100kc phase shifter in the output lead from the 100kc osc of the AN/URQ-11. This Ø shifter to be geared to suitable dials & of sufficient accuracy to be hand set to a/in 0.02 μsec. Suitable amplifier & emitter followers to be provided so output of Ø shifter can ~~be fed~~ feed the 41 timer & drive the hp-113BR freq divider and clock. Power for Ø shifter & hp-113BR clock to come from hp-724B standby power supply.

(b) Provide means so the clock output (positive 3μsec clock pulse from 113BR clock) can be used to reset the timer divider and with the same Ø code each time it is reset.

(c) Provide means to transmit a master pulse once per sec (as timed to drive clock pulse) and to occur 2.000 μsec before the 1st pulse of the master group (rate SØ)

to be done by Caroline Beale

(d) Coincidence alarm circuit to be built to indicate timer #1 & #2 not tracking together

must have to use 4 pulse next page →

② AN/FPN-38 timer

(a) Provide means for resetting the timer with a 2 sec (separate) pulse from hp-113BR clock so can reset timer if jump occurs or timer goes out (ie reset alt timer) back to a common reference & thus the master group will appear on the scope (in the service area) in the same relative position as it was before jump. (rate SØ)

(b) Alarm circuitry such that can determine when alt timer is not tracking operate timer to a/in 100μsec.

(c) Want this by 1 July, 1962 for Nº European Chain.

③ Monitor Function

2 separate receivers with clock etc & non-functions →

(a) For FPN-41 stations want to be able to monitor & cross monitor
clock #1 & timer #1
clock #2 & timer #2

(b) For FPN-38 want to monitor same as above.

(c) Time comparison monitoring:
FPN-41 Provide non function to get signal from WWV rcvr to time comparator (hp-114BR comparator) & to hp-160 scope. No WWV mon for FPN-38 stations

Summary of progress to 3/19/62: (AN/FPN-41)

① See p 22 and 23 for the block diagram of the proposed system to select a trigger for transmitting the "standard" second pulse. This pulse is to be transmitted in the "Z" interval, 2000 μsec ahead of the first pulse of the master group, occuring just after band nearest to the time of the standard second. The scope circuits to accomplish this are shown further on in this note book

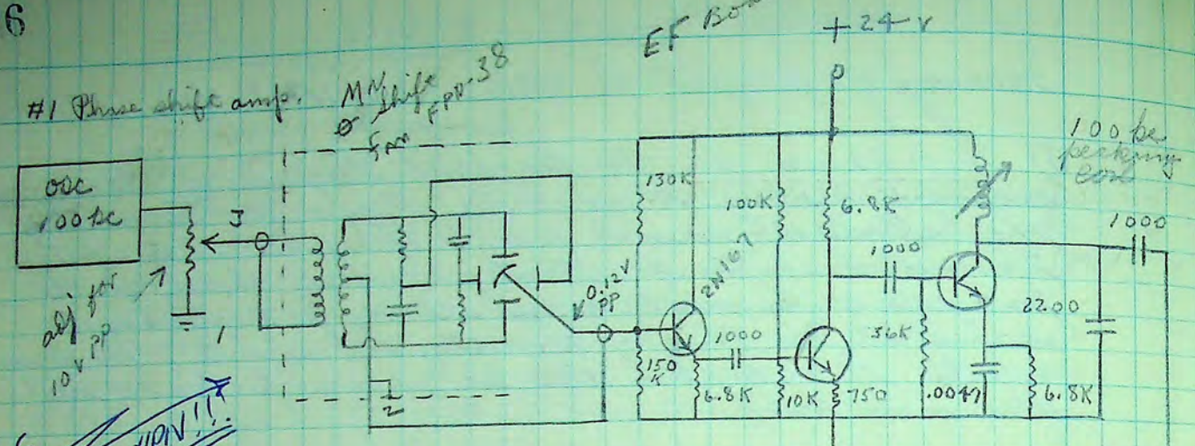
② The 3 μsec pulse from the hp-113BR clock will be used to generate a normal divider clear/reset pulse thru the existing 2021 divider clear/reset generator — various methods of inserting this pulse have been attempted with the following results (see page 26)

(a) injecting the 3 μsec pulse directly on the thyratron (ie pin 1 of V-18 in the divider drawer) without disconnecting the normal signal from V10B causes the desired reset but does not assure positive reset each time — the connecting of the 3 μsec pulse input cable to pin 1 causes the normal signals from V10B to be attenuated (ie shorted thru low R of cable) and allows the 3 μsec pulse to fire the 2021 — then when the 3 μsec pulse input is removed, normal trigger pick up the cancel reset — however, the amplitude of the 3 μsec pulse, thru about 24 feet of RG-59B/U cable, at pin 1 is about [redacted] 20 VOLTS and is not sufficiently large to insure positive triggering of the 2021 — It is felt that if the amplitude of this pulse can be increased to the neighborhood of 50 to 100 VOLTS, that positive reset/clear generation can be accomplished at the desired time and each time. (see p. 17)

see p. 20

(b) Several methods of increasing the 3 μsec pulse amplitude have been investigated including the use of a "one shot" multivibrator, blocking oscillator and trigger amplifier — design of such devices must include consideration of pulse delay (with respect to 3 μsec pulse input) and pulse rise time. These both must be kept to a minimum to retain desired timing of divider reset with the input 3 μsec clock pulse — The "one shot" and blocking oscillator circuits around

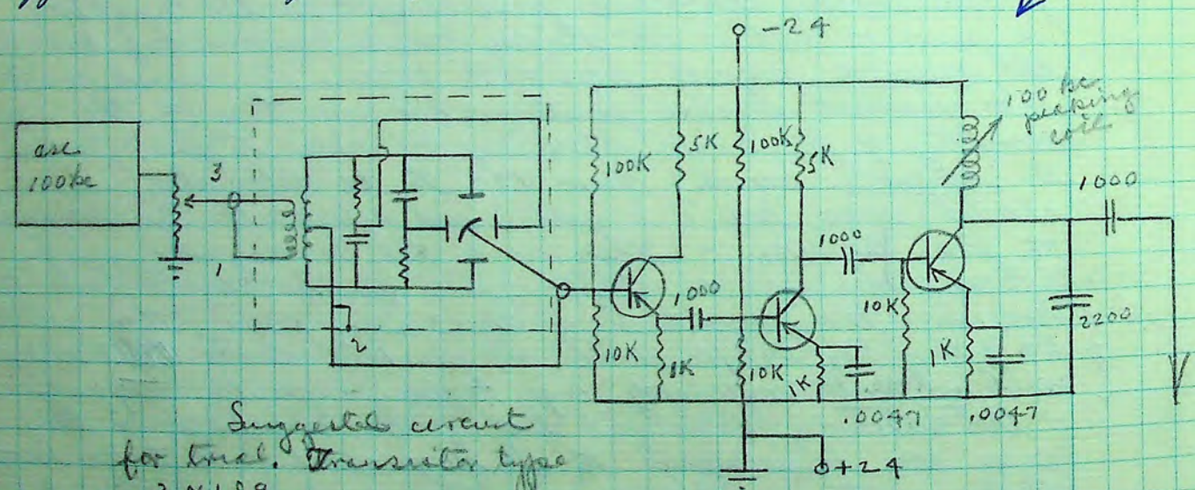
#1 Phase shift amp. MM shift FPN-38 from EF Board



N.G XPN!!!

Above not used due to potential of power supply and transistors.

Suggested 100KC amp to operate on VARIOGON & shifter OUTPUT



Suggested circuit for test. Transistor types
2N189
2N190
2N191
2N192

It are shown on pages 26 and 27.

(continued on page 18)

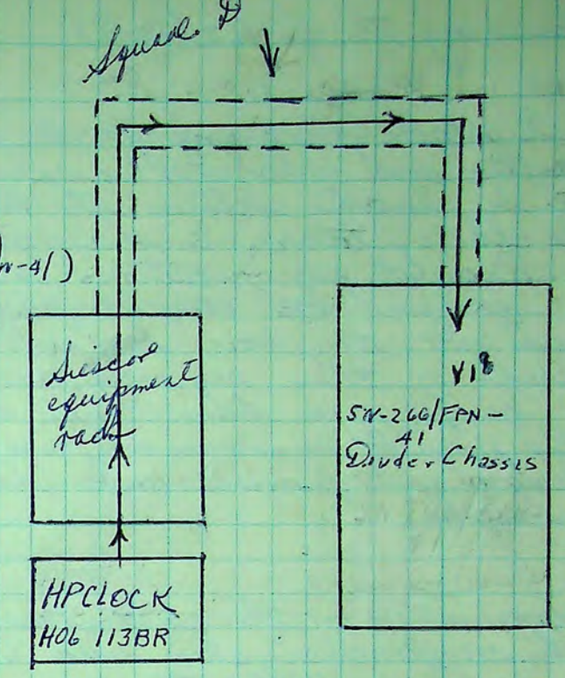
W234-

Phase I

Three cables to be run from HP clock to vicinity of V18 in sync drawer (FPN-41) chassis, 3 usec pulse from clock to V18.

Cables to be exact length in feet and inches.

Cables checked and made 24', 3 3/4 inches length.



Phase II.

Outline of setup as follows:

① 3μs pulse from clock fed to grid of V18 in sync divider drawer as per above drawing.

② Direct coupling to grid side of R-172 in drawer.

③ Voltage, amp and speed shown in Figs 1, 2 & 3 of pages 20 & 21.

Summary to 3/19/62 (cont'd):

③ A block diagram of the proposed 100KC phase shifter and associated amplifier/emmitter followers, etc to be placed between the 100 KC osc (URQ-11) and the clock/timer, is shown on page 28.

Requests for quotations on suitable phase shifters as well as complete packages including dial read out, etc; have been sent to several manufacturers — Results of these responses are filed in the project folder.

Design of a transistorized amplifier to be used in this project is shown on page 16 & 28. Further specific design will proceed when desired phase shifter is procured.

④ Information in this work-book prior to page 14 includes notes on familiarization with the Hewlett-Packard 113-BR divider/clock; 114-BR time comparator, 724-BR stand-by power supply and 160 oscilloscope. The charts shown will be used later to keep a record on oscillator/clock stability —

⑤ Block layout of the approximate timer room layout at Carolina Beach is shown on p 30

The proposed monitor junction dist. board is shown on page 30.

⑥ As a result of the meeting in H.Q. on 23 FEB 1962 — the following are the AN/FPN-38 requirements (BY 1 JUL 1962)

ⓐ Provide re-set facilities from clock (as per FPN-41) — except pulse occurs ea 2 sec

ⓑ Provide for use on rate SLO

ⓒ No 100KC phase shifter; no time comparator; no WWV receiver; no transmission of the standard second pulse

ⓓ Alarm system so that can tell upon 100 usec when opr & stand by timers not tracking.

(TURN TO PAGE 33) →

2/28/61

Mock set up normal operating currents:

Crystal oscillator CW 35044 type with one normal output J1401 meter readings as follows:

I_p	Osc out	60 μ amp.
	Pos 1	80 μ amp.
	Pos 2	100 μ amp
	Pos 3	100 μ amp
	Pos 4	95 μ amp
	Pos 5	100 μ amp.

Two outputs (one to mock up readings are as follows: (J1402)

Osc out	45 μ amp
Pos 1	80 μ amp
Pos 2	100 μ amp
Pos 3	100 μ amp
Pos 4	95 μ amp
Pos 5	104 μ amp.
	30

W-234. Loss or attenuation in trigger cable.

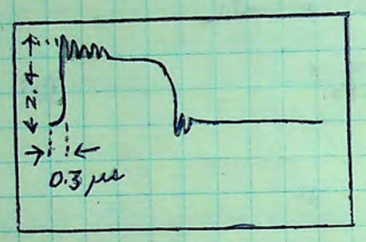
All cable 2.4 feet, 3 3/4 inches long.

Test #1 Rg-62B/U coaxial cable.

Pos. lick from H06-113BR clock fed into grid pin 1 of V18-2D21 of AN/FPN-41 Decimal chain.

90 Ω

Fig 1. 10v per CM

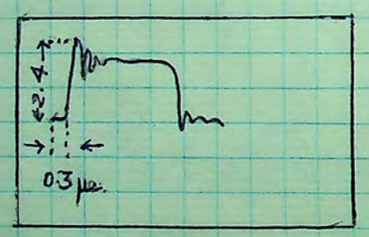


1μs per CM

Test 2. Rg 59B/U 72 Ω

10v per CM

Fig 2.



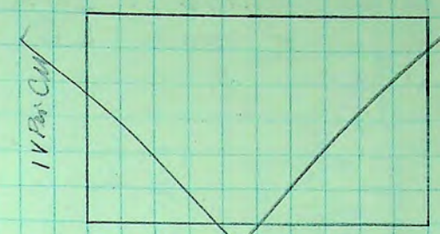
1μs per CM

below 0.3 μsec delay acceptable

No appreciable diff in #1 & 2 cables.

Test #3 RG-58C

FIG. 3



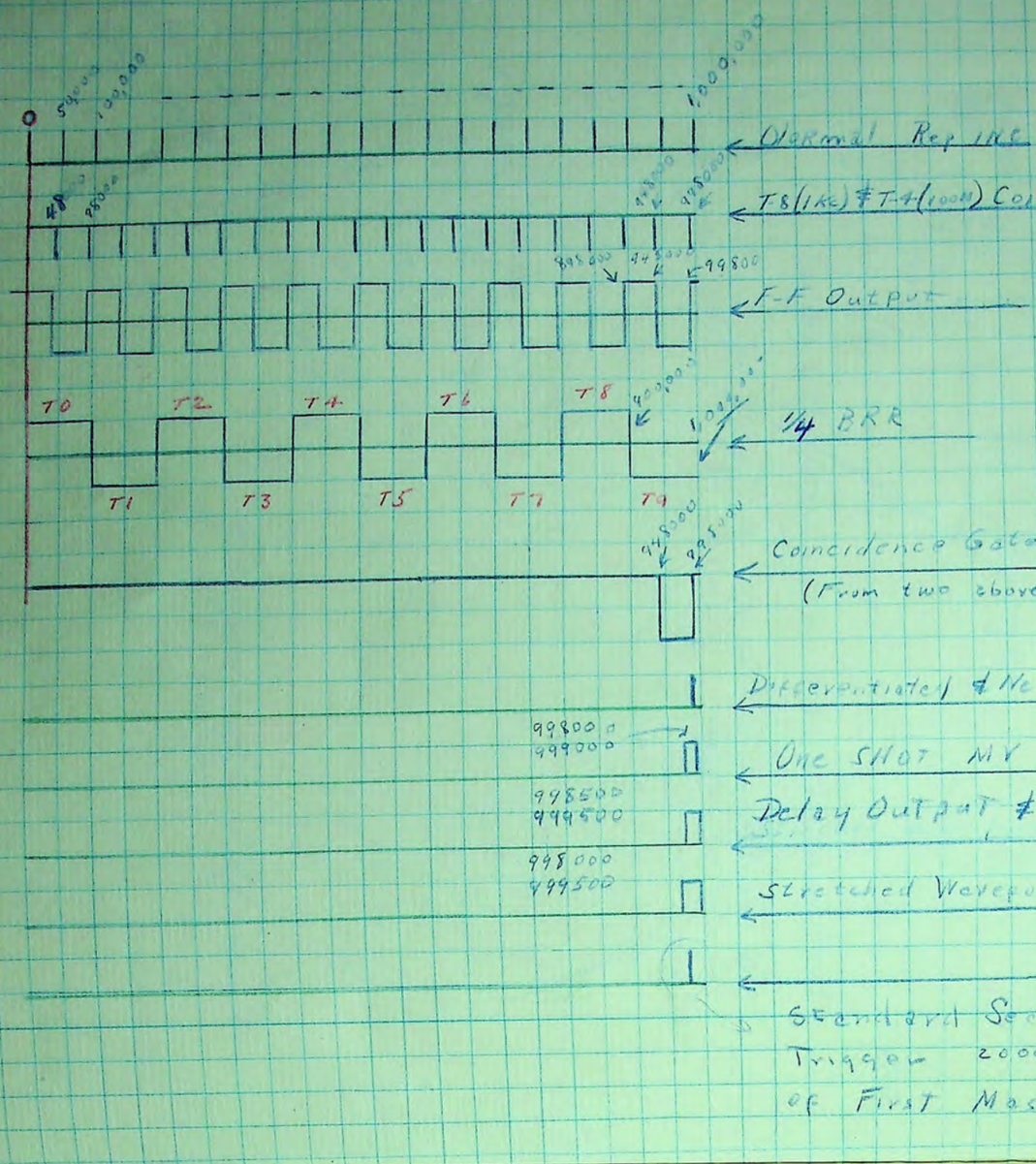
1μs per CM

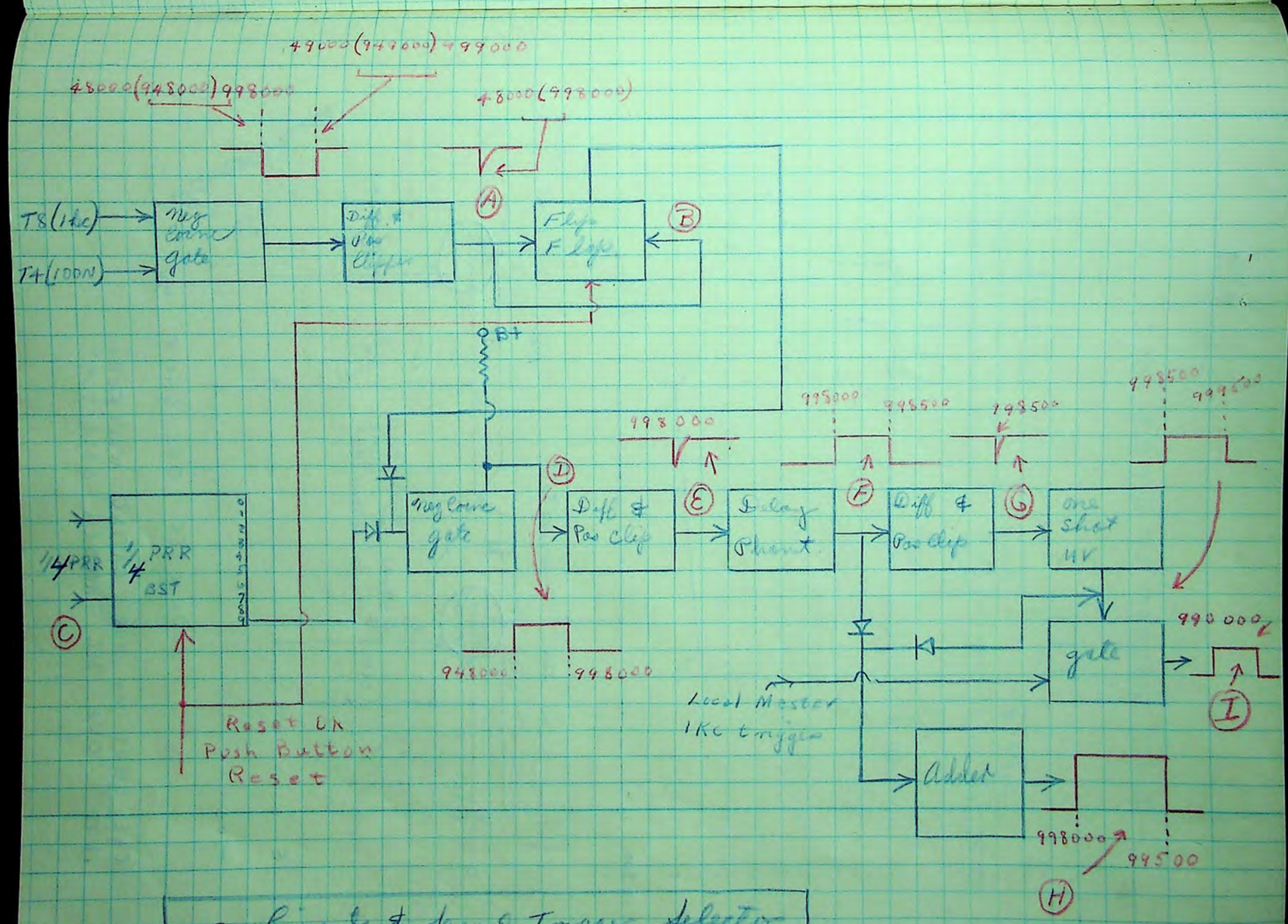
52 Ω characteristic impedance

Notes:

Probe used P6033 attenuation 10X.

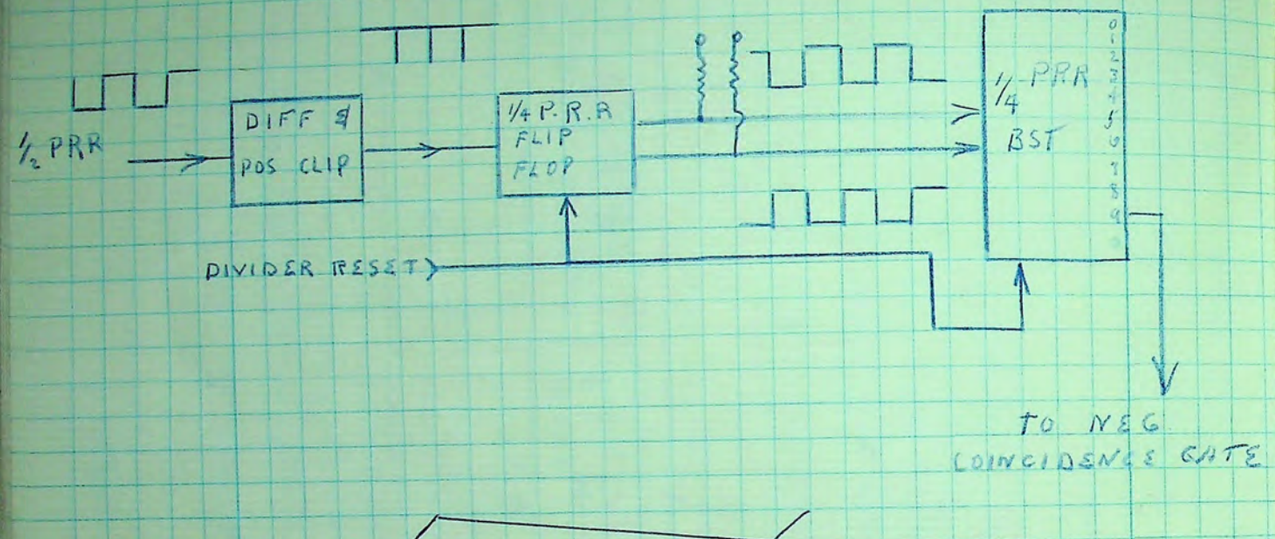
All waveforms made at P1 (grid) of V18 (2D21)

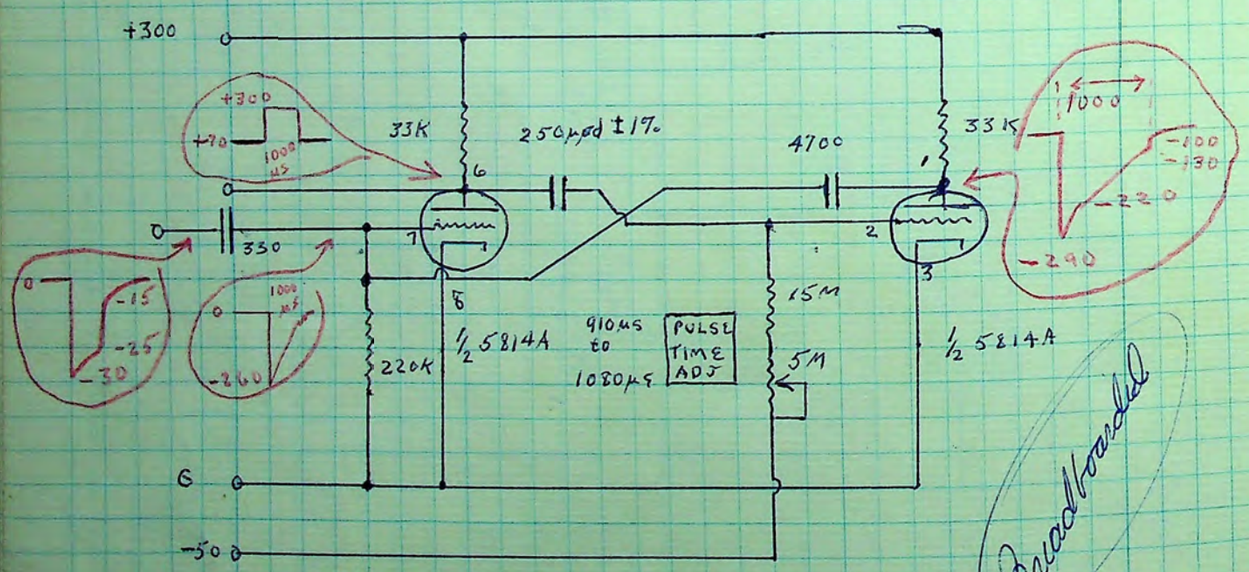




÷20 Circuit & Second Trigger Selector

BLOCK DIAGRAM OF 1/4 P.R.R. BST

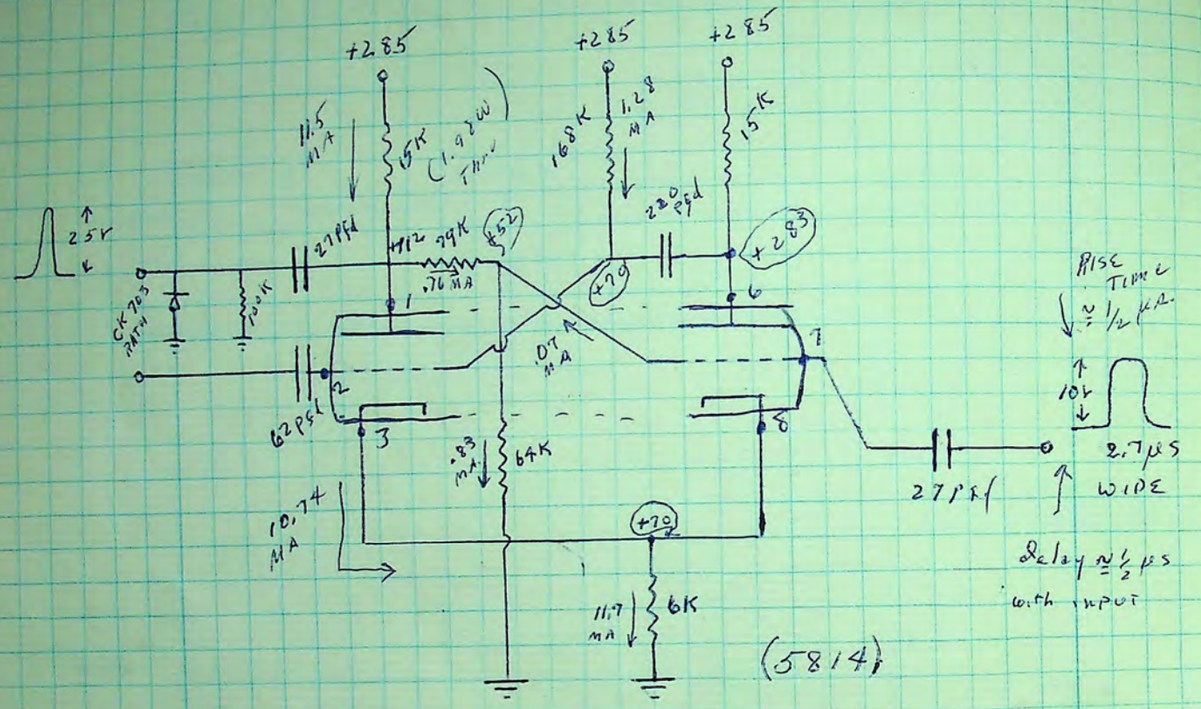




1000 μ SEC ONE SHOT MV

ONE SHOT MV FOR GATING WAVEFORM
INTO "ONE SEC TRIGGER SELECTOR"

ONE SHOT MV



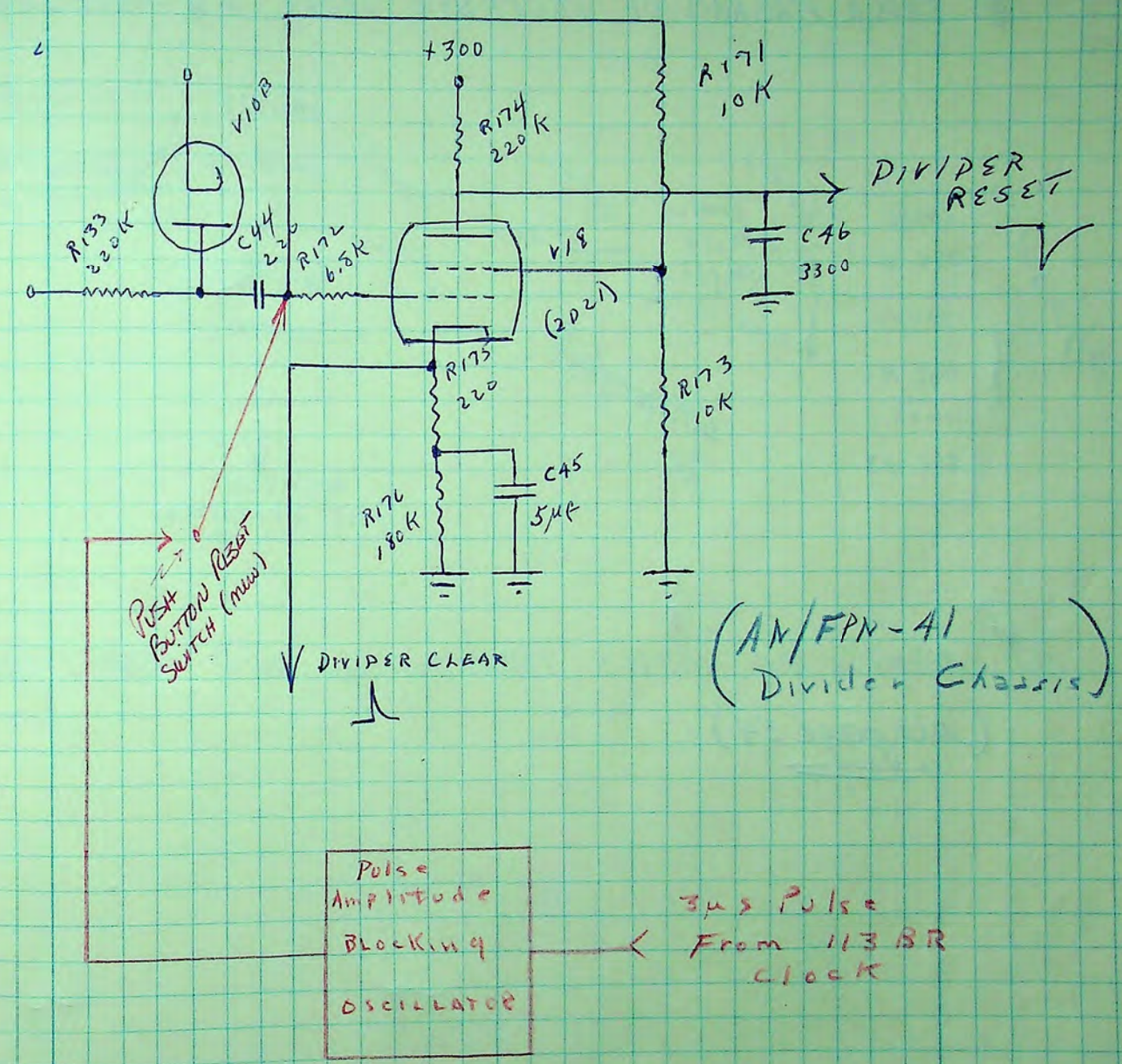
ONE SHOT TO GET HEALTHY RESET TRIGGER INTO DIVIDER RESET/CLEAR GENERATOR

COMMENTS

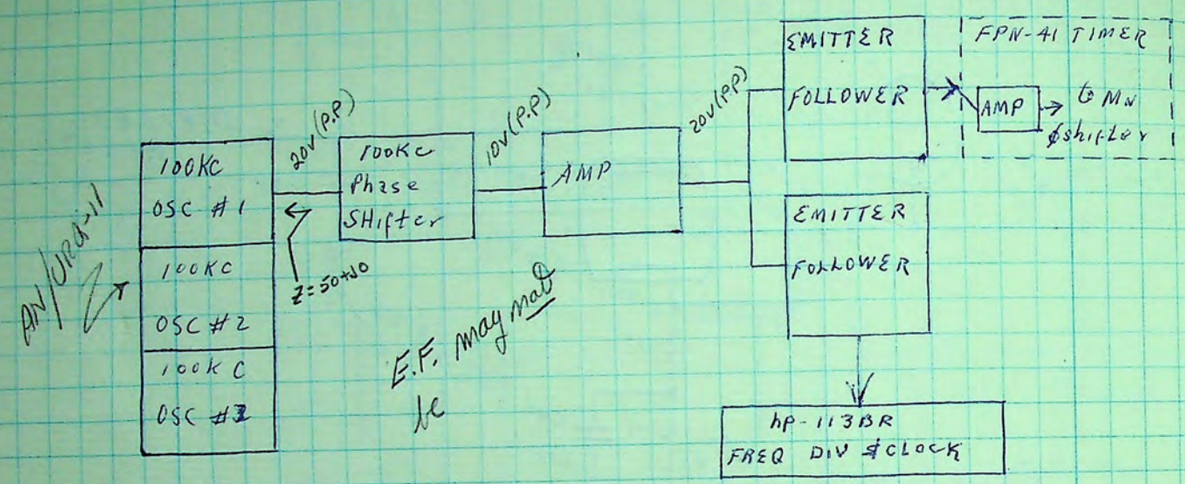
① Sacrifice output amplitude in attempt to achieve short rise time of output pulse with negligible delay.

② Load resistor on normally conducting half of tube (2W) gets very hot - circuit to inefficient to be used as desired.

DIVIDER RESET/CLEAR (PROPOSED)

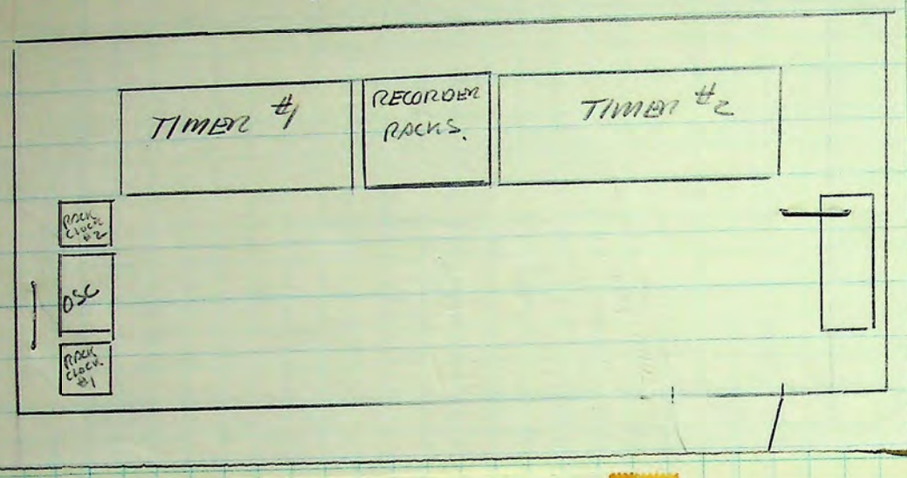


① BLOCK DIAGRAM OF PROPOSED 100KC + Ø SHIFTER

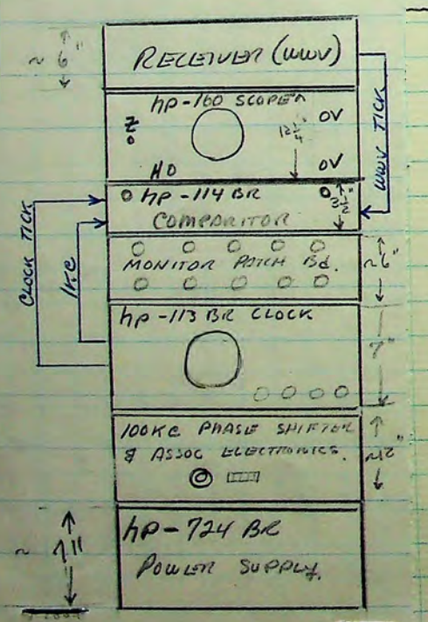


② SCHEMATIC OF 100 KC TRANSISTORIZED AMP (100KC) ABOVE
(see page 54)

APPROX: Carolina Beach timer room set up:

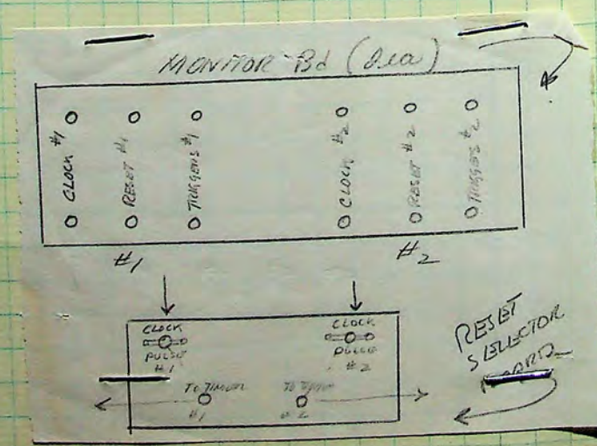


Proposed individual racks arrgmt



USE 1 6 RACK

0'-10"
1'-0"
0'-7"
0'-6"
0'-3½"
1'-¼"
0'-6"
2'-3 2¾" ≅ 5'

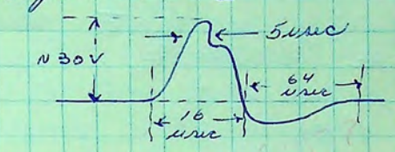


W-234 (cont'd):

3-19-62: DIVIDER RESET PROBLEM (CONT)

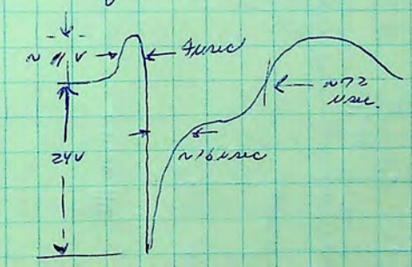
① Observed the FPN-41 operation of the blocking oscillators in the synch jitter-A and the "trigger amplifier" in the time sharing chassis to see if applicable to reset pulse from clock - interested in rise-time and delay perturbations.

② Signal into B.O. (disconnected) on input side of coupling capacitor C_2



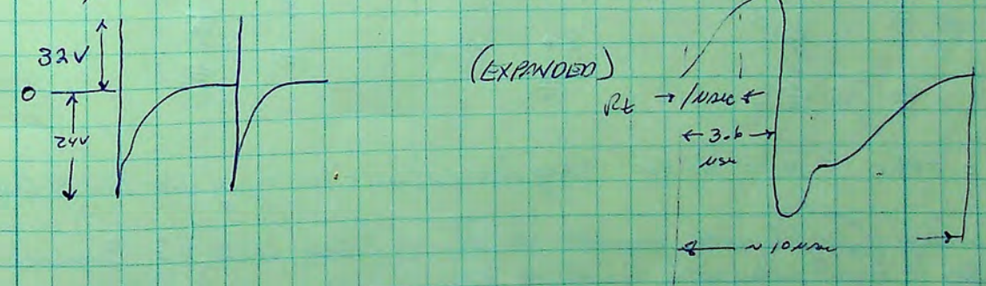
$R_t \cong 4$ usec

③ Reconnected C_2 to input of B.O. and observed waveform on input side of C_2 with B.O. functioning



$R_t \cong 3$ usec

④ Measured output (positive going) pulses from B.O.



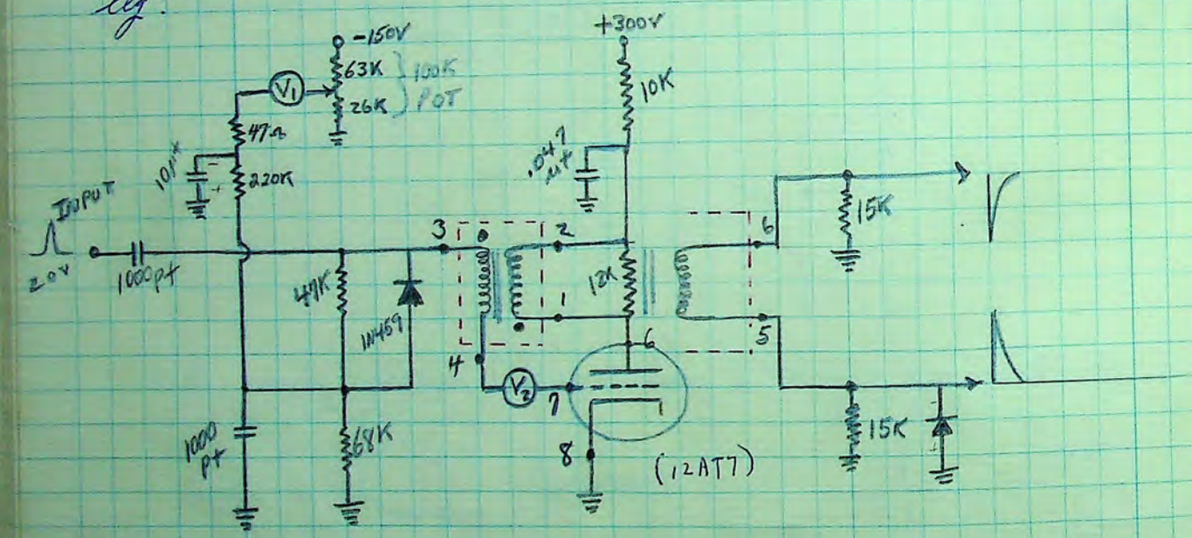
This type of circuit should perform to adequately boost the amplitude of the 3 usec clock pulse for firing the divider reset/clear thyratron (~~[illegible]~~)

W-234 (cont'd)

3-19-62 (cont'd)

Continuing to work with the 1/4 P.R.R. Beam Switch Tube and associated circuitry to give us the start of the basic waveforms in the "standard second" trigger selection circuitry — now have BST firing properly on the 1/2 PRR and intend now to construct a suitable 1/4 PRR flip-flop so can drive BST as desired:

Have the breadboard Blocking oscillator functioning as desired (see schematic ~~on page~~ BELOW ~~(2 and 3)~~). Because of the level of the 3 usec clock pulse into the B.O., it is necessary to decrease the negative 150V bias supply down to about 40 VOLTS using voltage divider in -150V leg:



(a) $V_1 = -68V$: $V_2 = -15.5V$ (any increase in -150V supply above this ↑ B.O. STOPS)

delay of OUTPUT pulse with respect to time ϕ (sweep start) ≅ 3 usec
delay of input pulse with respect to time ϕ (" ") ≅ 0.5 usec
rise time of output pulse (0 to +60 VOLTS) = 0.5 usec
" " " " " (0 to 110 VOLTS) = 1.5 usec

(b) $V_1 = -37V$: $V_2 = -8V$ (any decrease in -150V supply below this ↑ gives osc.)

delay of output pulse with respect to time ϕ (sweep start) ≅ 1.2 usec
input pulse delay " " " " " " " ≅ 0.5 usec

W-234 (cont'd)

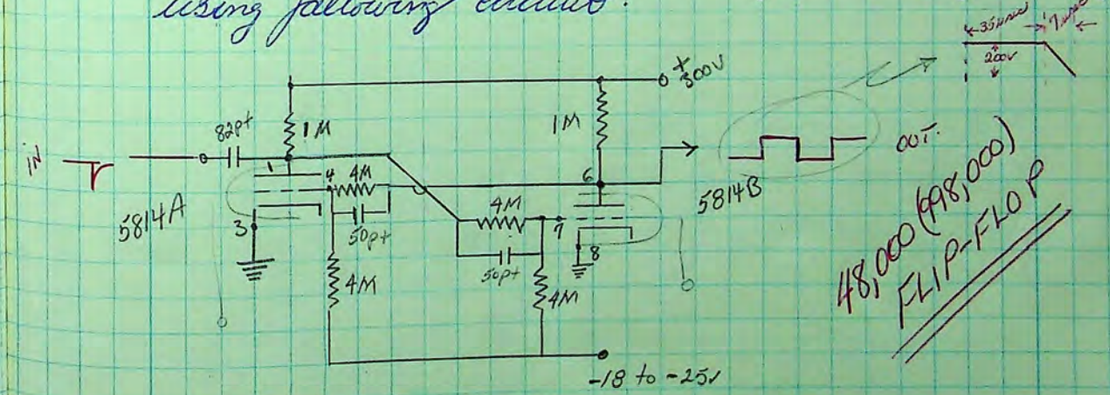
3-19-62 (cont'd):

rise time of the output pulse (0 up to +60 VOLTS) = 0.5 usec
" " " " " " (0 up to +110 VOLTS) = 1.5 usec

∴ under conditions of (b) or close thereto (ie V_1 = 40 VOLTS) we can get good stability of the pulses and not considering the delay in the run of the output pulse thru the probe and lead to the scope (estimated to be about 0.2 → 0.3 usec) The absolute delay of the output pulse with respect to the input pulse is approx 0.7 usec and the actual delay considering the run thru the probe to the scope, should be in the neighborhood of about 0.5 usec or so — this delay can be cranked out with the 113BR clock phase shifter —

3-20-62 : Fabricated and bench tested the blocking oscillator
3-21-62 on adjacent page — unable to properly test on timer due to "blank proper" work on equipment —

Breadboarded a flip-flop to operate on the d/f and positive clipped signals from the first Negative Comadinogate (ie T8 of 1K & T4 of 100 n info.) using following circuit:



3-22-62 :

An alternate methode to inject the one second standard pulse 2000 usec ahead of the master first pulse using the hp-113BR clock information direct is proposed on the attached sheets (next page) — this system, if it works, will be much less complex than the proposal on page 22 and 23 —

W-234 ALTERNATE PROPOSAL

① Assume the standard second pulse is on the air 2000 usec ahead of the first master pulse.

(a) Naval observatory monitors the local (master) transmissions and accounting for the predicted delay of the received pulse groups, determines the master station oscillator drift rate with respect to the observatory standard oscillator.

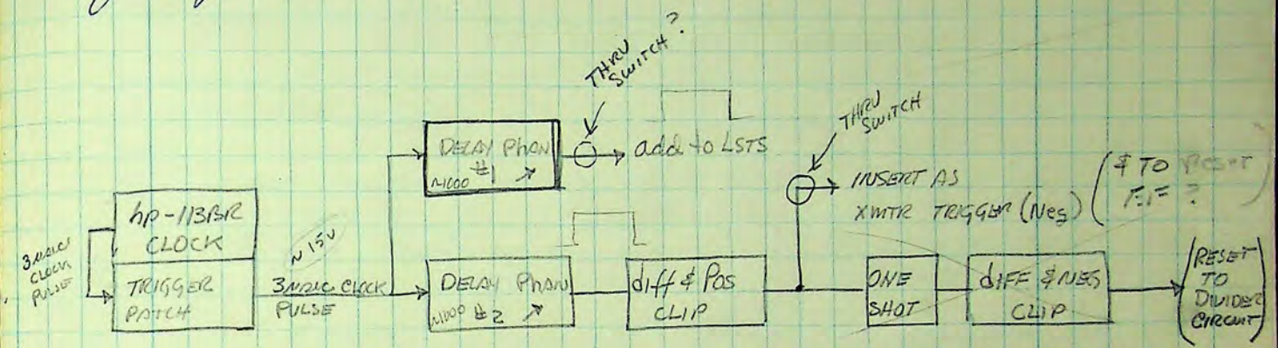
(b) Corrections to the master station oscillator are sent from the naval observatory and eventually the pulses received at the naval observatory exhibit some drift rate (+ & -) such that the mean is approx zero.

(c). After the drift rate is established and compensated for by corrections, the master group of pulses (and the transmitted standard second pulse) will appear on the naval observatory scope displaced by some amount of time from the accurance of the standard second as determined by the WWV clock. This displacement will include the travel time from the master station and some additional (or less) time which will be the error in time between the time of transmission of the standard second at the master station and the true time of the standard second at the master station.

W-234 (cont)

3/23/62 (cont):

This methode (opposite page) should require some electronics going into ONLY the divider (injection of reset), the transmitter driver (injection of a trigger and addition of a waveform to LSTS) and the switched attenuator (addition of waveform to LSTS)



delay phanistron #1: located in XMTR driver chassis (?) — to have a variable trailing edge (±500 usec) — to be triggered by a positive going pulse either from the clock direct or through the blocking oscillator already built.

delay phanistron #2: Also can be located in XMTR driver chassis (?) — to have a variable trailing edge adjustable to ±100 usec and to have a SHARP fall time on trailing edge — triggered as delay phan above.

one shot M.V.: To be located in divider drawer — to be triggered by a NEG pulse and put out a POSITIVE pulse to RESET SWITCH.

Before starting to construct the above plan to do the following as soon as timer is available

① Try to accomplish positive divider reset with clock pulse thru blocking oscillator as originally proposed in order to determine if this type reset is OK (since same principle going to be used in this new proposal)

cont.

(d) When the amount of correction in time is determined for the master station to transmit the standard second pulse at exactly the time of occurance of the standard second, the master station will be directed to advance (or retard) the 100KC phase shifter (between acc and clock/timer) by the necessary amount. This should bring into coincidence the master station standard second transmission and the actual time of the standard sec @ the master station.

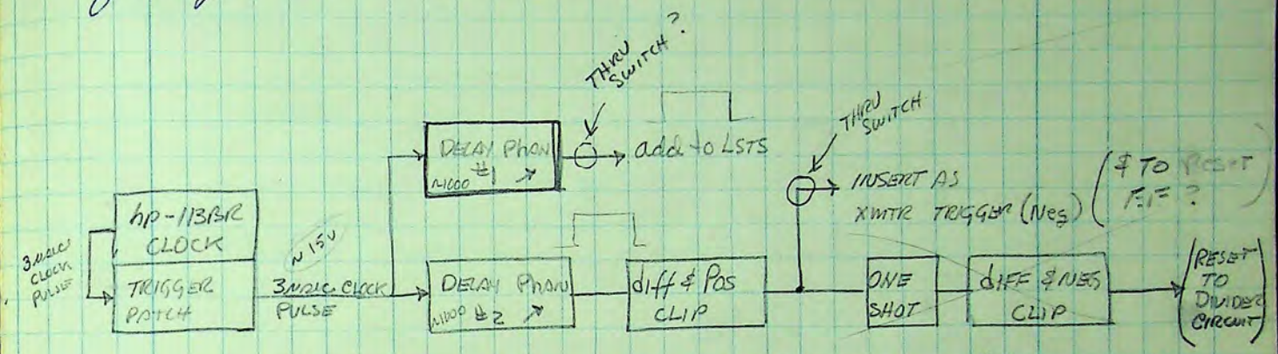
② At the master station, the time of occurance of the "3usec" 113BR clock pulse can be compared easily, to within 100 usec, with the time of receipt of the WWV time ticks using the hp-time comparitor. The dual trace capability of the hp-160 scope will permit time measurements between two waveforms to a higher degree of accuracy.

③ It is now proposed to simplify the method of inserting the one second transmission trigger 2000 usec ahead of the 1st master pulse (ie @ time of divider reset). This will cause the divider reset concurrently to change also from the earlier proposal. The new

W-234 (cont)

3/22/62 (cont): --

This methode (opposite page) should require some electronics going into ONLY the divider (injection of reset), the transmitter driver (injection of a trigger and addition of a waveform to LSTS) and the switched attenuator (addition of waveform to LSTS)



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one shot M.V.: To be located in divider drawer — to be triggered by a NEG pulse and put out a POSITIVE pulse to RESET SWITCH.

Before starting to construct the above plan to do the following as soon as timer is available

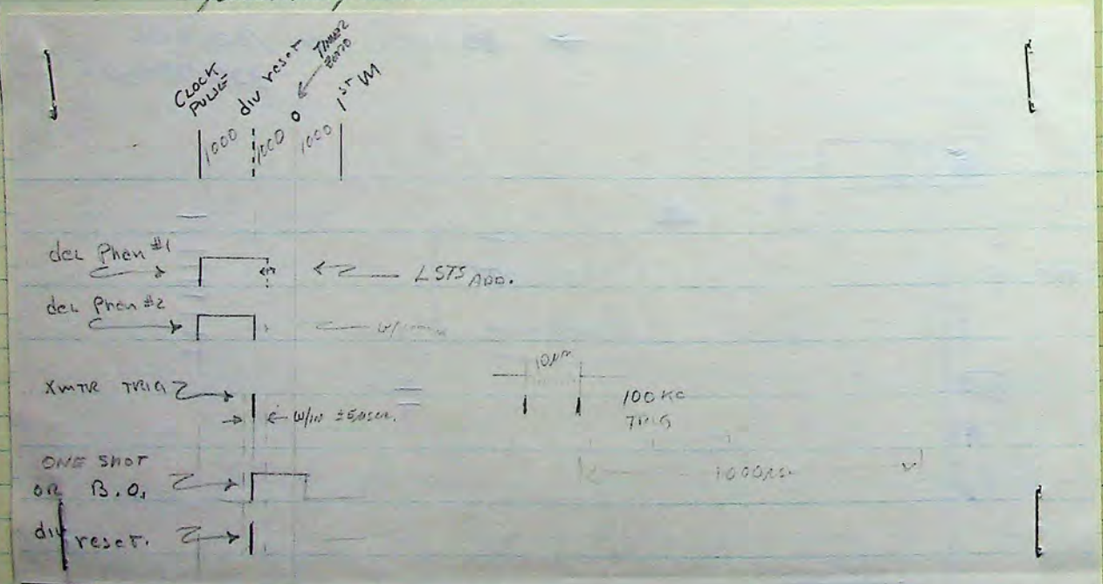
① try to accomplish positive divider reset with clock pulse thru blocking oscillator as originally proposed in order to determine if this type reset is OK (since same principle is going to be used in this new proposal)

cont.

proposal is as follows:

ⓐ since we have the capability of continuously phase shifting the HP-113BR clock output with respect to the 100KC driving the clock, we can move the 3usec clock pulse (or any pulse output) any desired amount. Since we do not use any time information from the clock (other than to run one sec) a delay of 1000 usec of the clock pulse with respect to the time of the standard second will be of little or no consequence.

ⓑ As proposed, they are to operate on the positive 3usec clock pulse in the following manner:

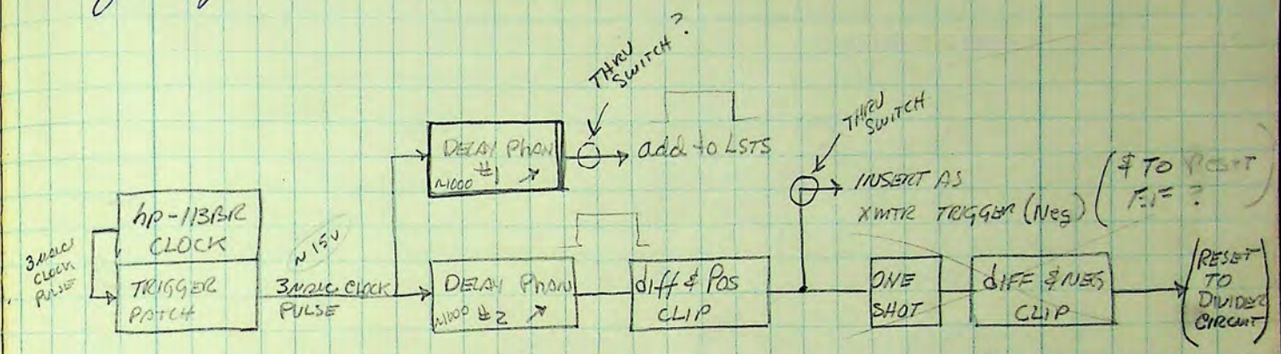


The 3usec clock pulse will go to two delay phanistrons (and perhaps through a

W-234 (cont)

3/23/62 (cont): —

This methode (opposite page) should require some electronics going into ONLY the divider (injection of reset), the transmitter driver (injection of a trigger and addition of a waveform to LSTS) and the switched attenuator (addition of waveform to LSTS)



delay phanistron #1: located in XMTR driver chassis (?) — to have a variable trailing edge (±500usec) — to be triggered by a positive going pulse either from the clock direct or through the blocking oscillator already built.

delay phanistron #2: Also can be located in XMTR driver chassis (?) — to have a variable trailing edge adjustable to ±100usec and to have a SHARP fall time on trailing edge — triggered as delay phan above.

one shot M.V.: To be located in divider drawer — to be triggered by a NEG pulse and put out a POSITIVE pulse to RESET SWITCH.

Before starting to construct the above plan to do the following as soon as timer is available

① try to accomplish positive divider reset with clock pulse thru blocking oscillator as originally proposed in order to determine if this type reset is OK (since same principle is going to be used in this new proposal)

3 cont.

blocking osc. first to gain pulse amplitude. Phanistron No 1 will produce a positive going wave form of approximately [illegible] usec duration and with an adjustable trailing edge (± ~500 usec) - This will be added to LSTS

Phanistron No 2 will produce a positive going wave form of very close to 1000 usec in duration and with control of the trailing edge to w/in about 100 usec. The trailing edge fall will be very rapid.

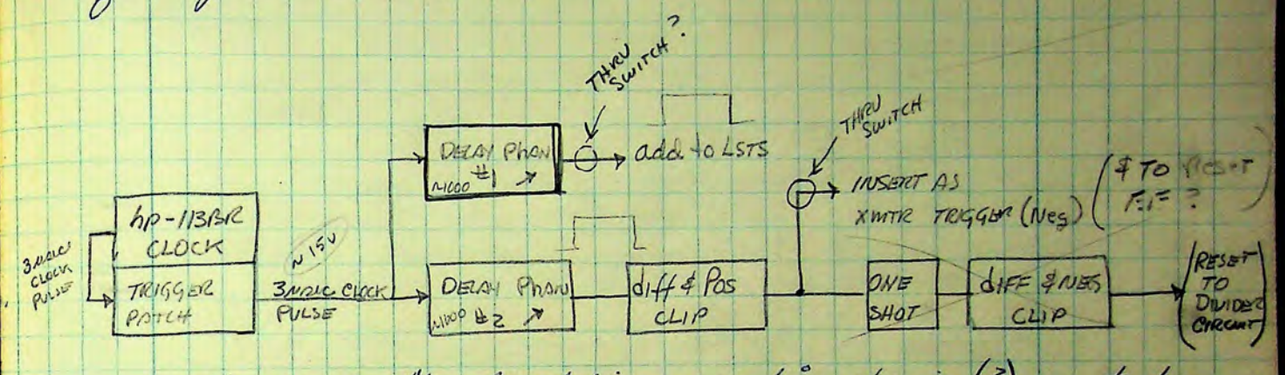
The trailing edge of phan #2 will be differentiated and applied as a negative trigger to the local multipulse train in the transmitter driver. This will become the "standard second pulse" trigger. This trailing edge will be used to trigger, also, a one-shot multivibrator or blocking oscillator.

The leading edge of the above one-shot will be differentiated and applied as the divider reset trigger (thru a push button switch) to the divider reset/clear generator in the divider drawer. The timing between the negative "std. sec" trigger and this reset trigger will have to be LESS than ± 5 usec

W-234 (cont)

3/22/62 (cont):

This methode (opposite page) should require some electronics going into ONLY the divider (injection of reset), the transmitter driver (injection of a trigger and addition of a waveform to LSTS) and the switched attenuator (addition of waveform to LSTS)



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one shot M.V.: To be located in divider drawer - to be triggered by a NEG pulse and put out a POSITIVE pulse to RESET SWITCH.

Before starting to construct the above plan to do the following as soon as timer is available

① Try to accomplish positive divider reset with clock pulse thru blocking oscillator as originally proposed in order to determine if this type reset is OK (since same principle is going to be used in this new proposal)

cont.

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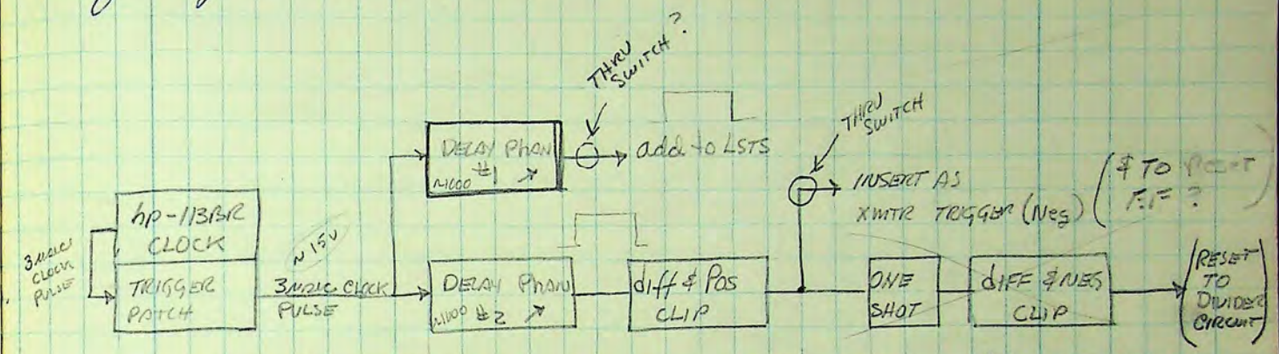
W-234 (cont)

3/23/62 (cont): -- --

This methode (opposite page) should require some electronics going into ONLY the divider (injection of reset), the transmitter driver (injection of a trigger and addition of a waveform to LSTS) and the switched attenuator (addition of waveform to LSTS)



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one shot M.V.: To be located in divider drawer - to be triggered by a NEG pulse and put out a POSITIVE pulse to RESET SWITCH.

Before starting to construct the above plan to do the following as soon as timer is available

① try to accomplish positive divider reset with clock pulse thru blocking oscillator as originally proposed in order to determine if this type reset is OK (since same principle is going to be used in this new proposal)

cont.

to insure that the proper 100KC transmitter trigger is selected in the transmitter driver. If this can be done, then the transmitted "std second" pulse will occur exactly 2000 usec ahead of the first master pulse and at the approx time of divider reset.

CONTROL →

By adjusting the trailing edge of the delay phanistron #1 waveform, the added LSTS interval can be controlled to insure proper operation of the switched attenuators.

By adjusting the trailing edge of the No 2 delay phanistron waveform, the standard second transmission can be inserted to properly occur 2000 usec ahead of the first master transmission

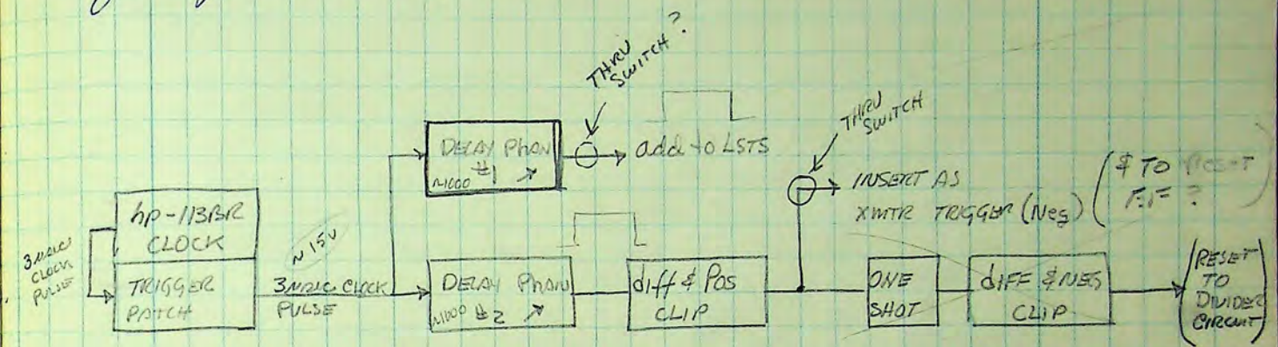
By Adjustment of the 100 KC phase shifter (between osc & timer clock), the relative position of the master group; standard second transmission, & all associated waveforms can be shifted together and steered to the exact time of the standard second

By adjustment of the φ shifter on the 1131BR clock, the one second pulse transmission (& LSTS added waveform and reset trigger) can

W-234 (cont)

3/22/62 (cont): → →

This methode (opposite page) should require some electronics going into ONLY the divider (injection of reset), the transmitter driver (injection of a trigger and addition of a waveform to LSTS) and the switched attenuator (addition of waveform to LSTS)



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one shot M.V.: To be located in divider drawer – to be triggered by a NEG pulse and put out a POSITIVE pulse to RESET SWITCH.

Before starting to construct the above plan to do the following as soon as timer is available

① Try to accomplish positive divider reset with clock pulse thru blocking oscillator as originally proposed in order to determine if this type reset is OK (since same principle going to be used in this new proposal)

3 cont.

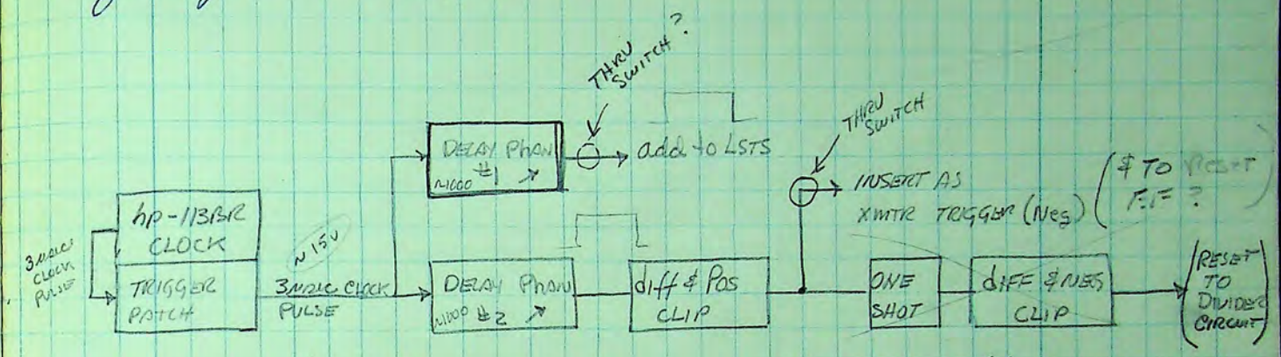
be shifted independent of normal timer operation and normal master group position. The one second pulses will shift in even 10 usec steps — divider used will be continuously shifted.

After moving the one second pulses transmitted anyplace in any interval, the divider can be "push-button" reset and the one sec pulses will fall back in 3000 usec ahead of the first master pulse —

W-234 (cont)

3/23/62 (cont): — —

This methode (opposite page) should require some electronics going into only the divider (injection of reset), the transmitter driver (injection of a trigger and addition of a waveform to LSTS) and the switched attenuator (addition of waveform to LSTS)



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one shot M.V.: To be located in ~~[illegible]~~ divider drawer — to be triggered by a NEG pulse and put out a POSITIVE pulse to RESET SWITCH.

Before starting to construct the above plan to do the following as soon as timer is available

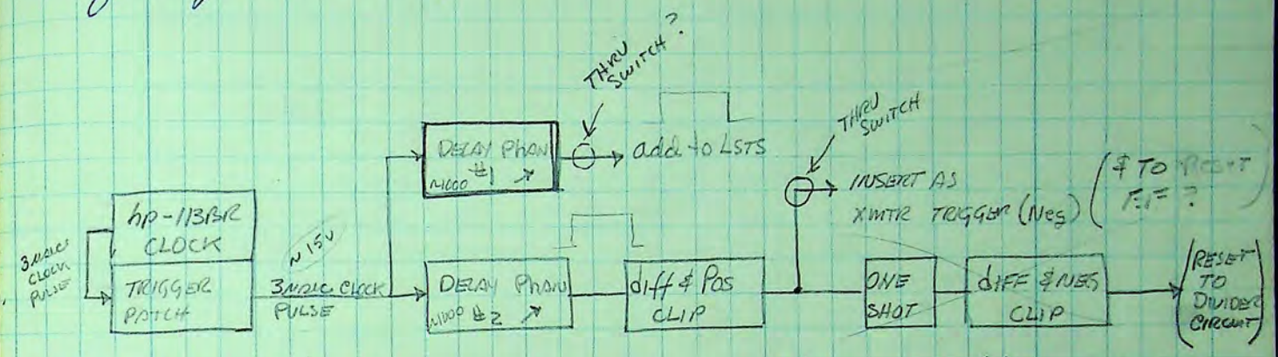
① try to accomplish positive divider reset with clock pulse thru blocking oscillator as originally proposed in order to determine if this type reset is OK (since same principle is going to be used in this new proposal)

3 cont.

W-234 (cont)

3/22/62 (cont) : -- --

This methode (opposite page) should require some electronics going into ONLY the divider (injection of reset), the transmitter driver (injection of a trigger and addition of a waveform to LSTS) and the switched attenuator (addition of waveform to LSTS)



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one shot M.V. : To be located in ~~[illegible]~~ divider drawer — to be triggered by a NEG pulse and put out a POSITIVE pulse to RESET SWITCH.

Before starting to construct the above plan to do the following as soon as timer is available

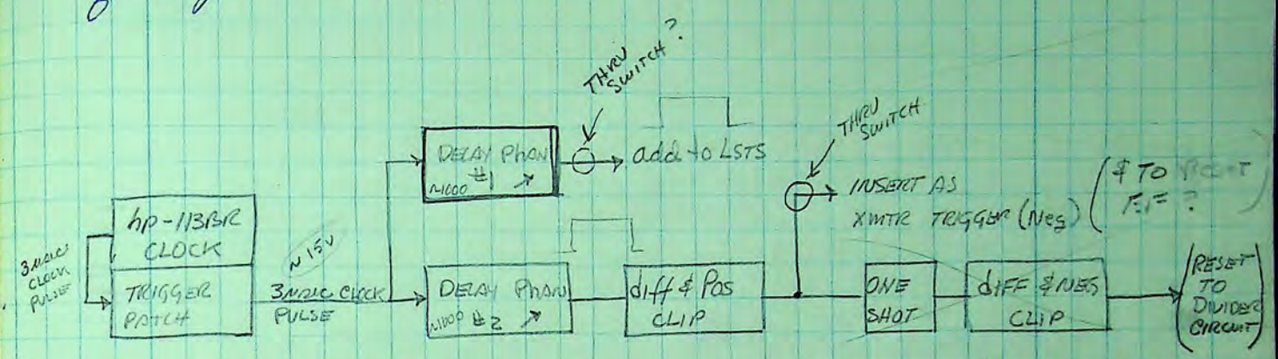
① Try to accomplish positive divider used with clock pulse thru blocking oscillator as originally proposed in order to determine if this type of reset is OK (since same principle is going to be used in this new proposal)

} cont.

W-234 (cont)

3/23/62 (cont) : -- --

This methode (opposite page) should require some electronics going into ONLY the divider (injection of reset), the transmitter driver (injection of a trigger and addition of a waveform to LSTS) and the switched attenuator (addition of waveform to LSTS)



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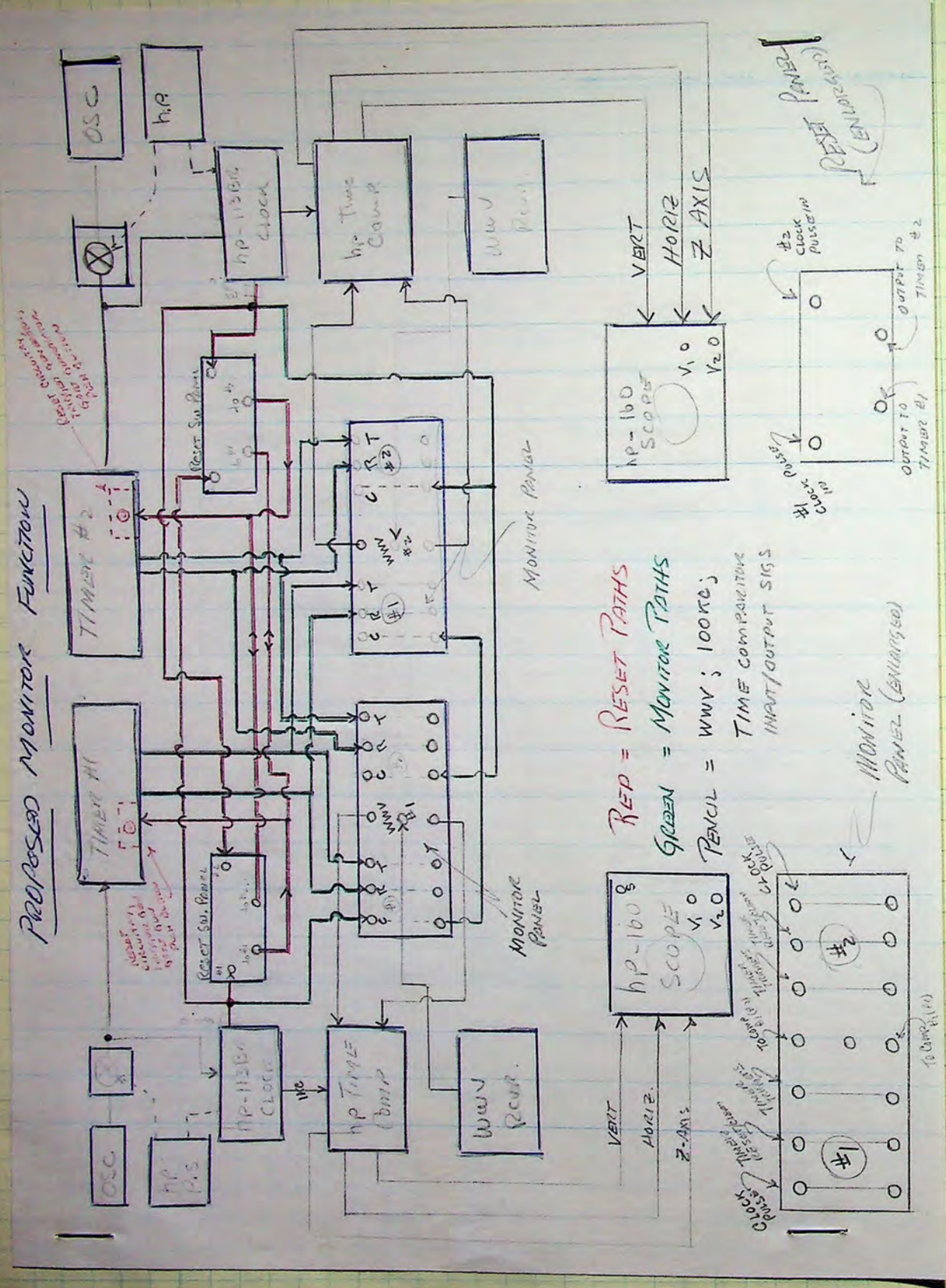
one shot M.V. : To be located in ~~[illegible]~~ divider drawer — to be triggered by a NEG pulse and put out a POSITIVE pulse to RESET SWITCH.

Before starting to construct the above plan to do the following as soon as timer is available

① try to accomplish positive divider reset with clock pulse thru blocking oscillator as originally proposed in order to determine if this type of reset is OK (since same principle is going to be used in this new proposal)

} cont.



W-234 (cont'd)
3/22/62 (cont'd)

② Thoroughly investigate the existing (and proper) timer wave forms and ground paths to insure:

(a) That the injection of LSTS can be conveniently done on XMTR driver and slotted attenuator without feeding back thru timer

(b) That the "std sec" trigger injection is properly done to avoid adverse feed back

(c) That the new circuitry can be inserted in existing timer drawers as desired and avoid adverse heating & crowding effects — to keep signal paths to a minimum — etc.

The various BNC connectors and fittings ordered for the monitor function came in today and the monitor panel has been ordered cut to specs. This work will not proceed until can get back on the timer next week —

also investigation continuing on suitable delay phanestron for use in the new proposal (last page).

3/23/62:

Investigation of available space in the AN/FPN-41 timer indicates that all of the associated electronics in this new proposal for std. sec insertion and reset (ie both #1 & #2 delay phanestron, one shot M.V., etc) would best fit into the transmitter driver drawer. The "reset" push button will go either on the front of the "divider drawer" or on front of the "transmitter driver drawer"

The proposed monitor panels and their interconnection diagram between timers #1 & #2 are shown on the adjacent (←) page.

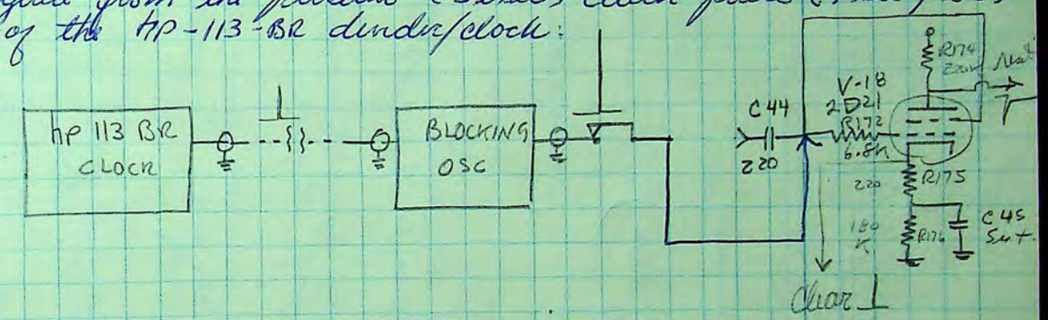
Mounted monitor panel in equip (temp) rack and made up several short BNC patch cords for use on this. Made up "reset panel" ready for mounting —

W-234 (CONT)

3/26/62: Timers tied up with "blink" tests – proceeding with the monitor panel installation & hook up

Running 100KC from URQ-11 to clock (with snaff cable slack to permit connection to phase shifter in the future) – also running separate 115V a.c from URQ-11 power to prevent overload of timer room strip receptacles:

Commenced wiring in the proposed blocking oscillator (see p. 34) to furnish a positive trigger thru a momentary contact switch to the 2D21 in the divider chassis. The purpose of this test will be to see if the positive pulse actually will properly reset the timer divider – The blocking oscillator will be triggered from the positive (3 usec) clock pulse (1 sec prr) out of the HP-113-BR divider/clock:

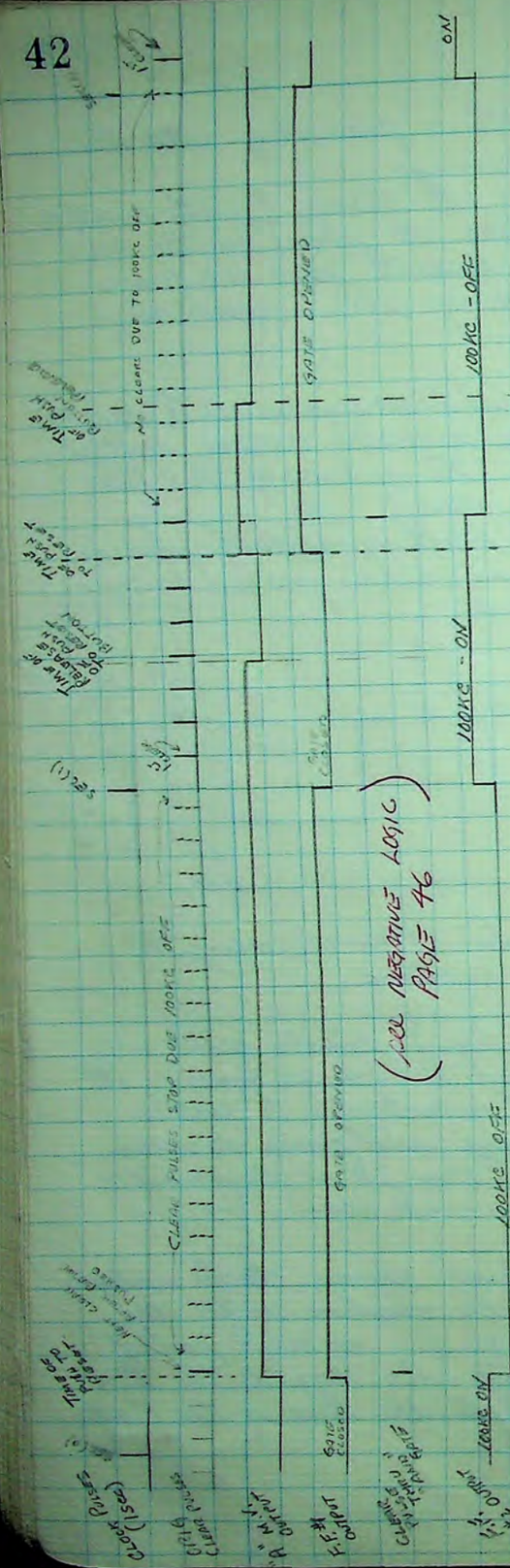


3/27/62: Attempted to reset the timer divider (FPN-41) using the above methode – ran into trouble as follows:

① As long as the initial (existing) divider reset is displaced appreciably (ie more than 20 to 30,000 usec), it is possible to reset the divider (sporadically) to within ±1000 usec. But as soon as the existing reset comes to within 20,000 usec or so of the clock pulse, then it is impossible to reset the divider – ie Random reset occurs –

② A closer look at the timer divider shows that random reset will be the rule and not the exception with the above proposed method -- ie, depending on what part of the divider count that you reset will depend the time relation of actual reset as compared to the time of the clock pulse used to reset –

(OVER)



(see NEGATIVE LOGIC PAGE 46)

① Just before the "reset button" is pushed, the divider is counting normally and producing positive going "divider clear" pulses (ie divider clear/reset gen.)

② On pushing the reset button, a positive going waveform is applied to the "AND GATE" and the "4 F.F." is changed in state to (+) and allows the "gate" to open.

③ With the "gate" opened, the positive clear pulses can reach the "AND GATE" and thus get through since a (+) going waveform is also present at the gate. This positive clear pulse (ie, the first one after reset button is pushed) goes on to F.F. #2.

④ F.F. #2 then changes state (due to + clear pulse above) and provides an inhibiting waveform to block the 100KC input to the divider - ie turns divider OFF.

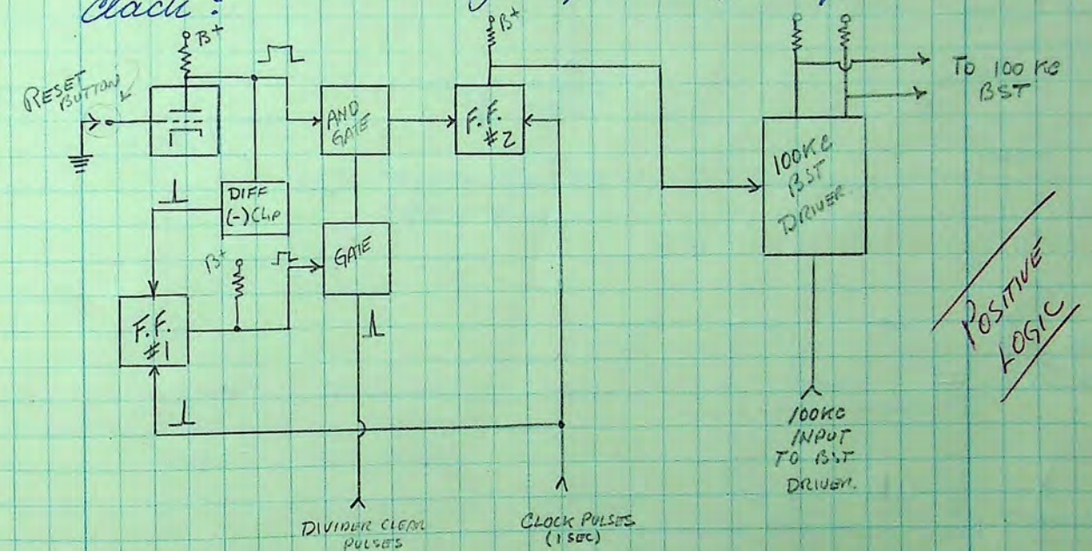
⑤ The divider should now have been cleared, reset and stopped waiting for a signal to continue counting out.

⑥ When the "clock pulse" is received on the second, F.F. #2 changes state and 100KC is permitted to enter the divider and divider continues counting. The second clock pulse also causes "GATE" to close F.F. #2 the one the new clear pulses are blocked.

W-234 (cont'd)

3/27/62: (CONT): CONCLUSION: On discussion of the problem with Mr Jenny and Mr Landus, the conclusion was reached that the direct methode of divider reset will not work properly and assure a reset close enough to time Ø to be considered a good coarse reset: It was further concluded that the only positive way to insure a good divider reset would be to stop the divider chain - set everything to zero and then start the divider on receipt of a reset pulse train -

The following is proposed to accomplish a workable, coarse divider reset using a positive pulse from the 113BR clock:



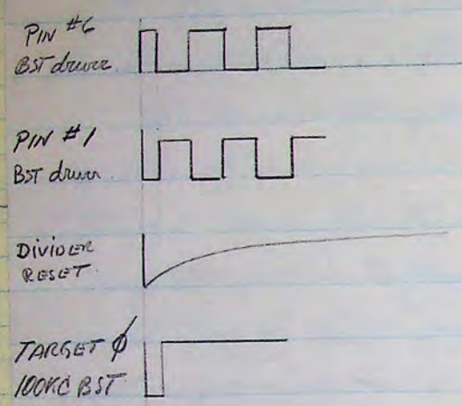
Refer to waveforms on the opposite page to see how the above circuit operates:

① "divider clear" (+ going) and "one second clock pulses" (from HP-113BR clock) are continuously fed into the circuit:

② The output is an inhibiting waveform going to the 100 KC BST driver (proposed) to control starting and stopping of divider chain.

③ The "push to reset" button just grounds the grid of the tube to turn it OFF & produce a (+) going waveform.

100KC BST-DRIVER (F.F.) & WAVEFORMS.



① At the time of divider reset, the beam is formed on spade #9 of the 100KC-BST and immediatly shifted to spade #0 by the positive going output from pin #6 applied to odd switching grid of the BST. The beam will stay on spade zero (with negative target zero output) until the signal from pin 6 goes negative (at some time from one to 10 usec later) at which time the beam is switch to spade #1 & the target zero output goes positive.

② Will want to HOLD (INHIBIT) the plate (pin 6) of the BST driver POSITIVE immediatly upon the reset so that the BST will hold with the beam formed on target ϕ — ie can do this by holding waveform positive(?) at point where divider reset enters.

t=ϕ,

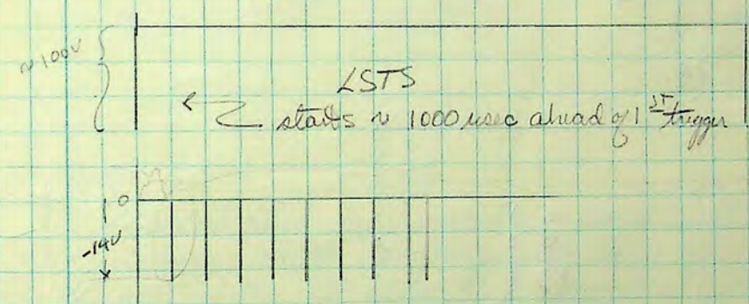
W-234 (CONT):

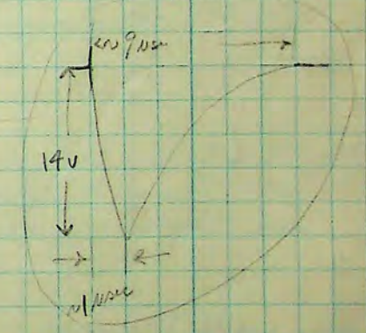
3/28/62

Investigated the FPN-41 divider, 100KC BST driver and its action upon normal reset of the divider chain. A discussion of the action and the proposed necessary "inhibit" waveform to stop the divider immediatly upon reset is shown on the opposite page —

Proceeding with design and breadboard of this new method to obtain "one second" timed, timer reset.

Investigating the FPN-41 local selected, multiple trigger coming into the transmitter driver chassis to determine their time relation with LSTS and their characteristics so that similar waveforms of trigger can be developed for the "standard second" trigger insertion.





These are the negative transmitter triggers (at input to XMTR DRIVER) in FPN-41

Timing of LSTS w/resp to XMTR trigger is shown.

Re: page 42 and new divider reset scheme — investigating now the possible use of all negative logic to simplify gates and flip-flops —

Called Mr STOBBE at Pulsar Mfg company in regards to their telegram re info. on the 100KC phase shifter and mechanical package — see long distance phone call sheet —

③ At the time of the clock timing pulse, we will want the inhibit pulse to be removed and one of the two additional actions to take place:

(a) remove the positive inhibit pulse from the grid of the "A" side (pin 2) and let the next 100KC (negative) trigger cause the "A" side to cut off (and thus allowing the plate (pin 1) to go positive) and the plate of the "B" side (pin 6) to go negative — thereby switching the beam from spade 0 to spade 1 — etc for normal continuation of divider function

(b) or remove the positive inhibit pulse as described above and at the same time, hit the "B" plate (pin 6) with the negative going half of the #2 F.F. causing immediate switching action of the BST from spade 0 to spade 1 — this may not be desirable if injection of the negative waveform from #2 F.F. could interfere with normal BST & divider operation

t=0,

W-234 (CONT):

3/28/62

Investigated the FPN-41 divider, 100KC BST driver and its action upon normal reset of the divider chain. A discussion of the action and the proposed necessary "inhibit" waveform to stop the divider immediately upon reset is shown on the opposite page —

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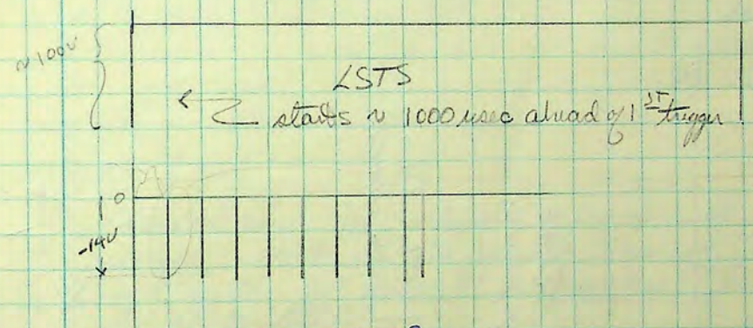

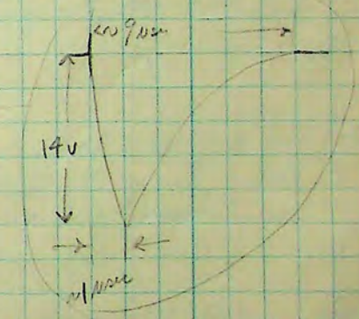

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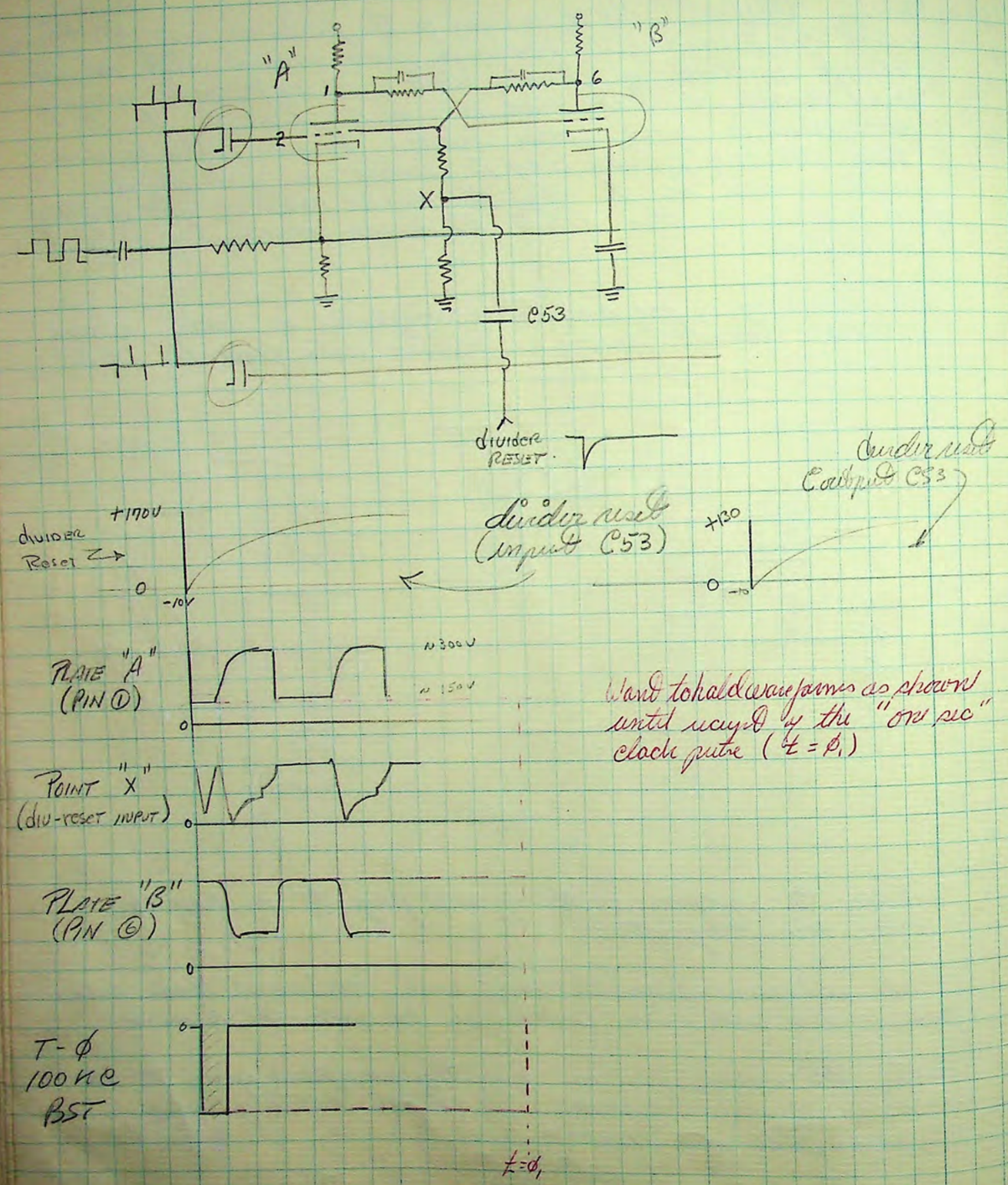

Want to hold waveforms as shown until keyed by the "one sec" clock pulse ($t = \phi_1$)

W-234 (CONT):

3/28/62

Investigated the FPN-41 divider, 100KC BST driver and its action upon normal reset of the divider chain. A discussion of the action and the proposed necessary "inhibit" waveform to stop the divider immediately upon reset is shown on the opposite page —

Proceeding with design and breadboard of this new method to obtain "one second" timed, timer reset!

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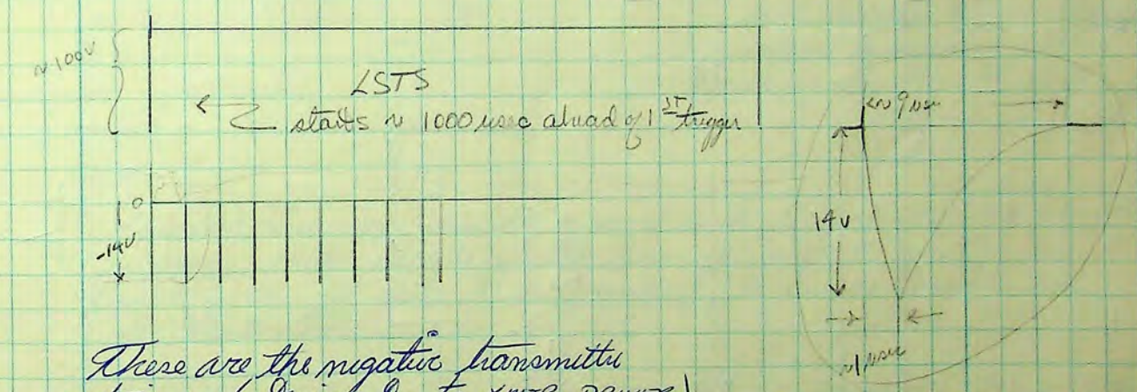

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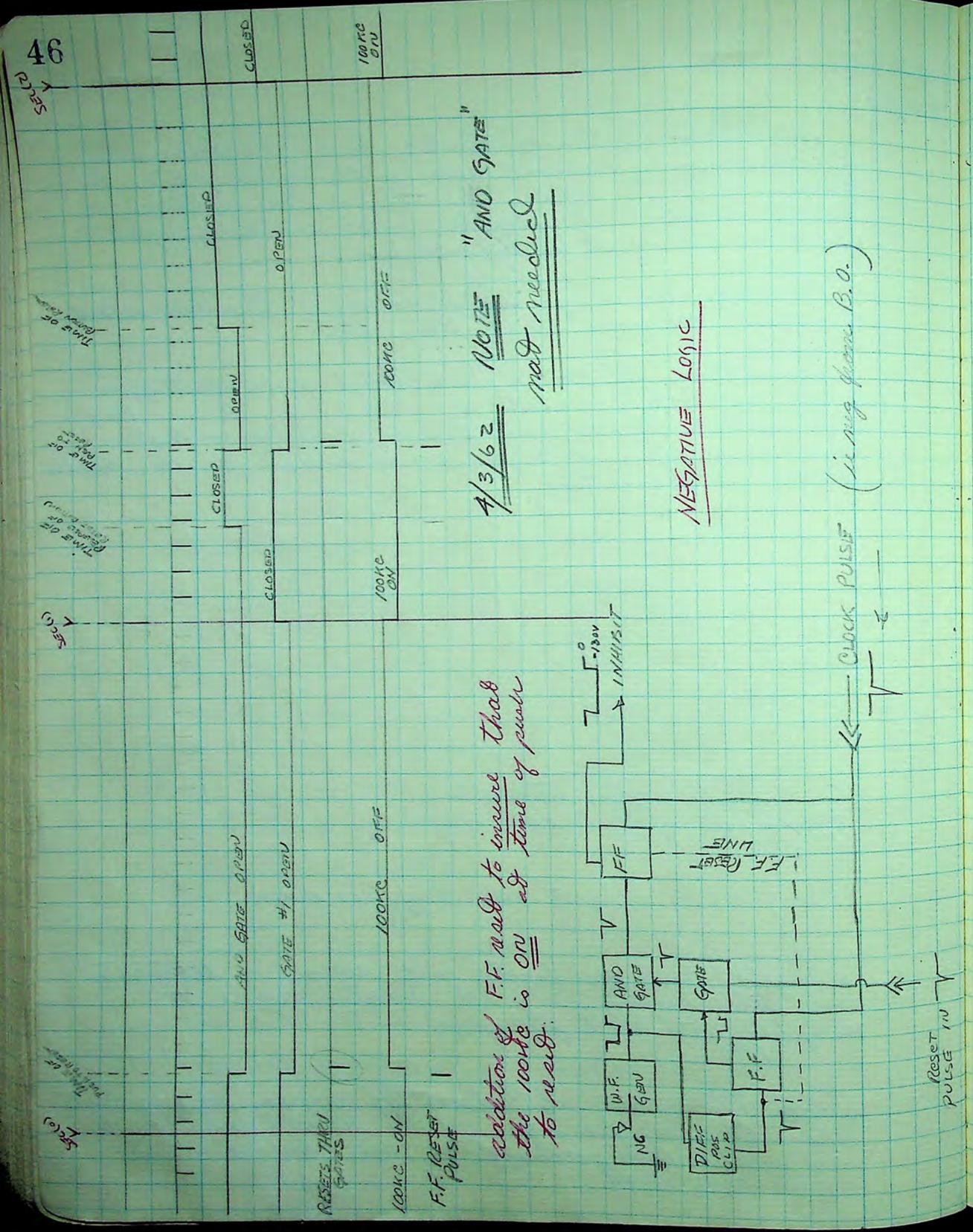


4/3/62 NOTE "AND GATE" not needed

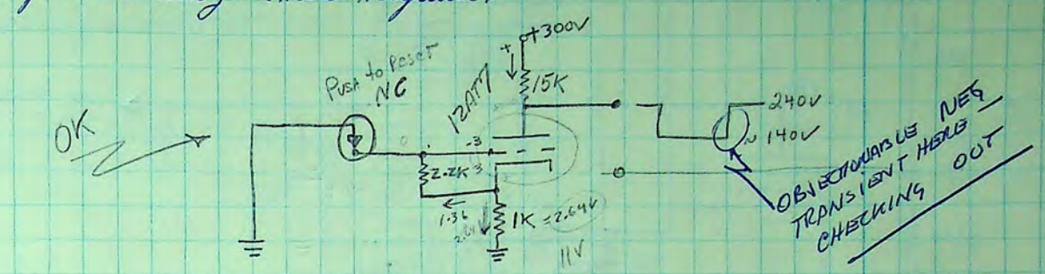
NEGATIVE LOGIC

addition of F.F. reset to insure that the 100KC is ON at time of push to reset.

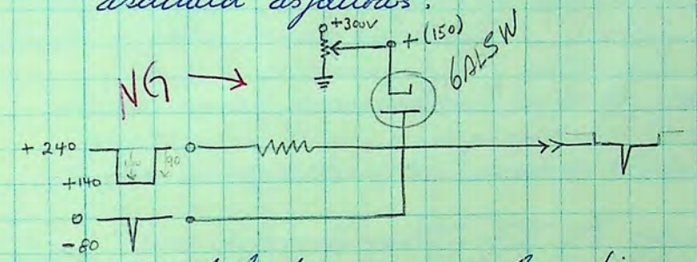
W-234 (cont):

3-29-62

Commencing to fabricate, on bread board, the "push to reset" waveform circuitry (now negative)



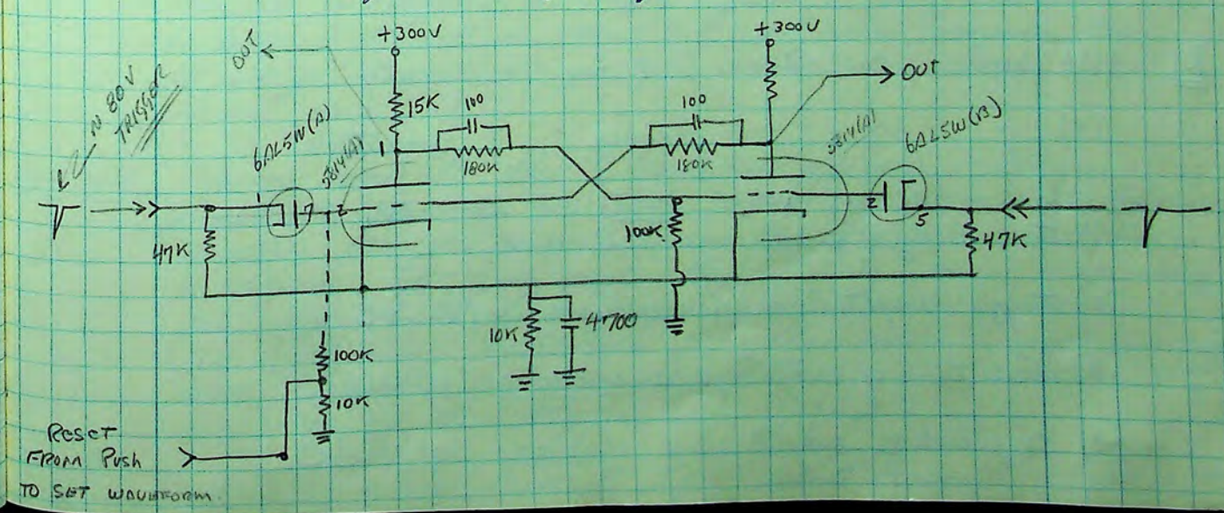
To test the proposed "and gate", will use above output waveform plus the negative output from earlier built blocking oscillator as follows:



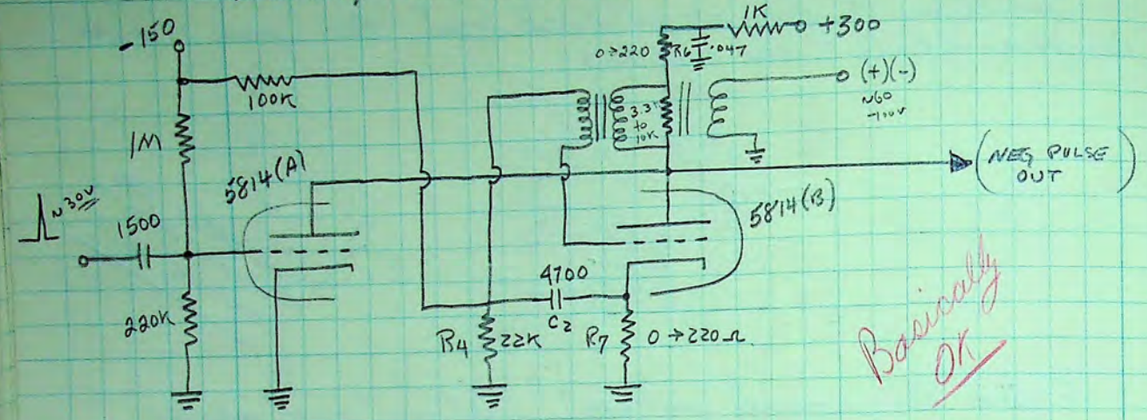
Also want to differentiate and positive clip the above waveform to trigger the 1st F.F.

decided also may need a firm reset signal to #2 FF to insure that at the exact time of "push to reset", the state of the F.F. output is positive to insure 100KC "on" at that time:

Plan to use following flip flop M.V. from 41 timer board.



BLOCKING OSCILLATOR CIRCUIT (revised):



Basically OK

C_2: (1) as large as possible to minimize the voltage change during the pulse and permit the transformer to determine pulse width

(2) return to ground to get ~ 10% decrease in pulse width

R_4: (1) may be as low as desire commensurate with required power dissipation

(2) control of grid circuit time constant

R_6: (1) increase here causes increase of pulse width } small effects

(2) " " " " " " " amplitude

R_7: (1) increase here causes increase of pulse width

(2) " " " decrease " " amplitude

SHUNT CAPACITANCE ACROSS XFMR. MUST BE KEPT TO MINIMUM AS:

(1) time delay of pulse increases w/ shunt C

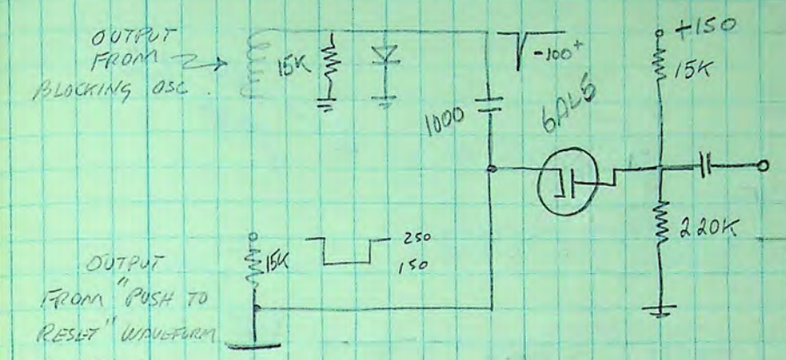
(2) trigger amplitude needs increase w/ shunt C

(3) rise time of output pulse increases w/ shunt C

(4) amplitude of output pulse decreases w/ shunt C

3-30-62:

Continuing with construction (breadboard) of "and gate" — design on p. 48 unstable & N.G. for levels of waveforms — tested below proposed gate using neg signal from previously built blocking oscillator.



NG

Results: encouraging — gate seems acceptable — going ahead now with breadboard of F.F. to see what variations in trigger level acceptable for triggering F.F. with trigger thru above gate: (see F.F. circuit on last page ie page 47)

4-2-62 Some difficulty getting F.F. to operate (found wiring error) — operation satisfactory but delay of the trigger out of the Blocking oscillator (ie w/respect to input clock trigger) is about two (2) microseconds and this could cause trouble later in initiating the 100 KC flip-flop in time to positively stop the divider chain operation with the 100 KC BST from formed on spade Φ. —

Therefore investigating a more refined Blocking oscillator in the attempt to reduce this delay and also improve the output pulse rise (decay) time — see B.O. circuit on opposite page (48) ←.

4-3-62 going back to the "standard second" trigger insertion circuitry — (see p 37) — if can use the negative trigger, generated from the delay phase. #2 waveform, to give me the timing pulse necessary for the reset flip-flops, then there should be less delay problems — this may (and probably will) require some amplification and perhaps C-F isolation of this trigger —

Also in going back to the "reset circuit" (see p. 46)

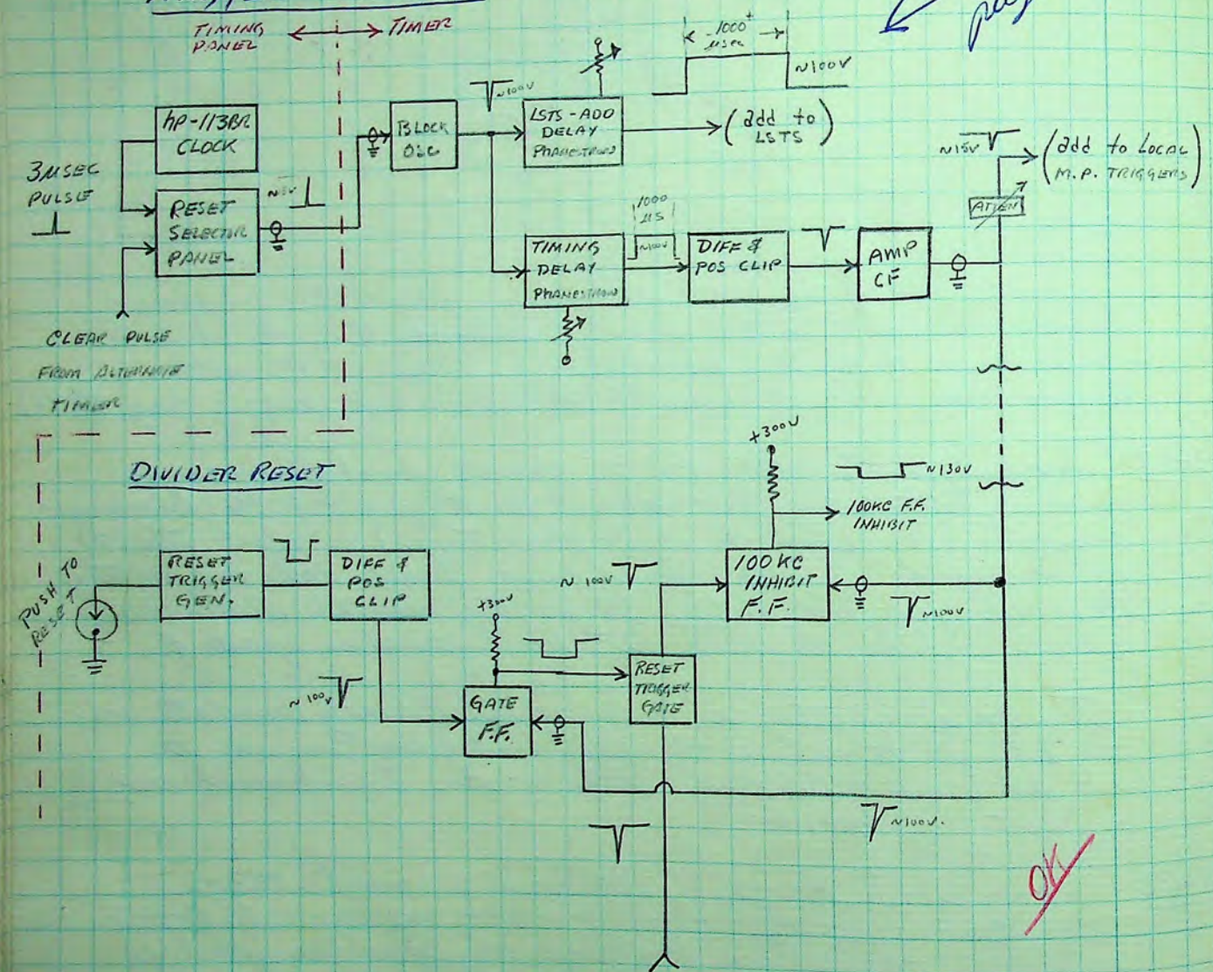
#4675.00 left for {W-232, W-234}

4/3/62 (CONT):

the "AND GATE" is extra baggage and not needed to properly gate out a divider reset trigger and still block out the input reset after the 100KC F.F. is inhibited — therefore the two revised circuits are as follows —

TRIGGER INSERTION

see page 62



OK

W-234 (cont'd)

4/3/62:

Carried out the fabrication of the following shielded delay phantastron to the lab to be tried in conjunction with the trigger insertion circuitry —

"DELAY PHANTASTRON CIRCUIT"

(AS IN WORKS)

Changes — see more schematics ↑ page 124

Received quotation from NILSEN Co on phase shifter package (585.00 ea) — called Bastian & Said go ahead on order of package — ordered 4/4/62

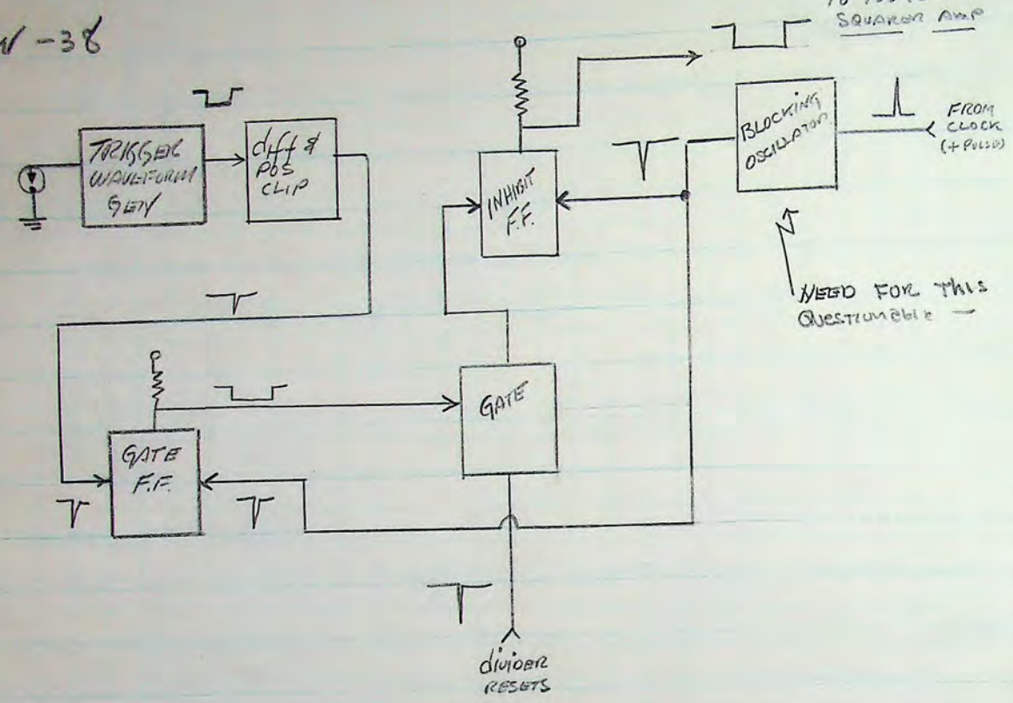
4/4/62 Still working on B.O. (see p 48) trying to get a fast rise time and a reasonably narrow pulse — finally achieved desired results taking negative out put from the plate of the 5814 (B) in lieu of those the transformer output terminals —

Commencing to assemble together the first few stages which have been developed — ie the B.O., trigger reset generator; gating F.F. and the diode gate

Commenced detailed investigation into the AN/FPN-38 timer dividers to determine the methods of reset — decided that the basic reset system as designed for the FPN-41, can be used. Inhibiting is planned for the 100KC square amplifier with normal divider reset coming in, as in the FPN-41, and the dividers stopped on reset to be started again with the next clock timing pulse — see general block diagram on next page 3 (p 51)

AN/FPN-38 TIMER — PROPOSED RESET CIRCUIT

FPN-38



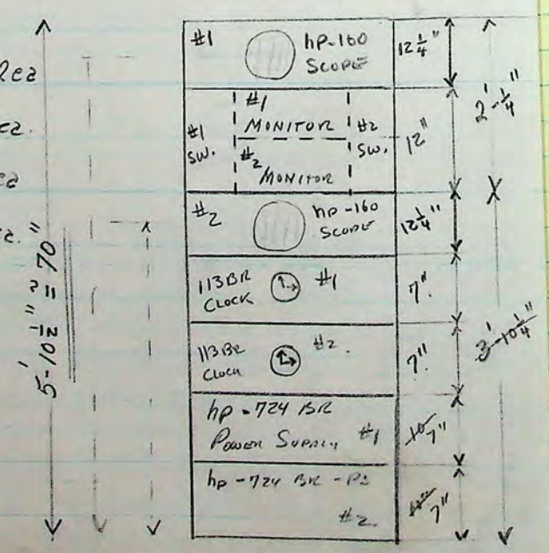
MONITOR/SWITCHING FUNCTION:

(a) HP-113BR (HO7) FREQ DIV/CLOCK - 2ea

(b) HP-160 SCOPE - 2ea.

(c) SIGNAL MONITOR PANEL - 1ea

(d) SWITCHING PANEL - 1ea.



ordered 70" (inside) high rack with solid side panels - rear door - blue in color - on 4/4/62 →

W-234 (CONT) —

4-5-62: Completed fabrication of a 100KC amplifier to be used in conjunction with the phase shifter (being procured from NILSEN MFG. Co) - see schematic on next page (54) -

The two racks for the FPN-41 timing project equipment arrived today - supports for inside are on order — plan to mount one in timer room as soon as all assemblies are here & as personnel available to do this —

Continuing with breadboarding & interconnection of the basic reset & trigger insertion circuitry as already fabricated in stages —

4-6-62: Send VARIGON 100KC phase shifter (from spares) to lab for mounting on a board with the 100KC amplifier already built — plan to connect this into one of the present clock set ups to check the amplifier operation: signal levels available for both the clock and the timer (thru ~20' of coax cable) and operation — may need E.F. outputs so plan to check this too:

Continuing with testing of divider reset / trigger insertion modules for proper operation —

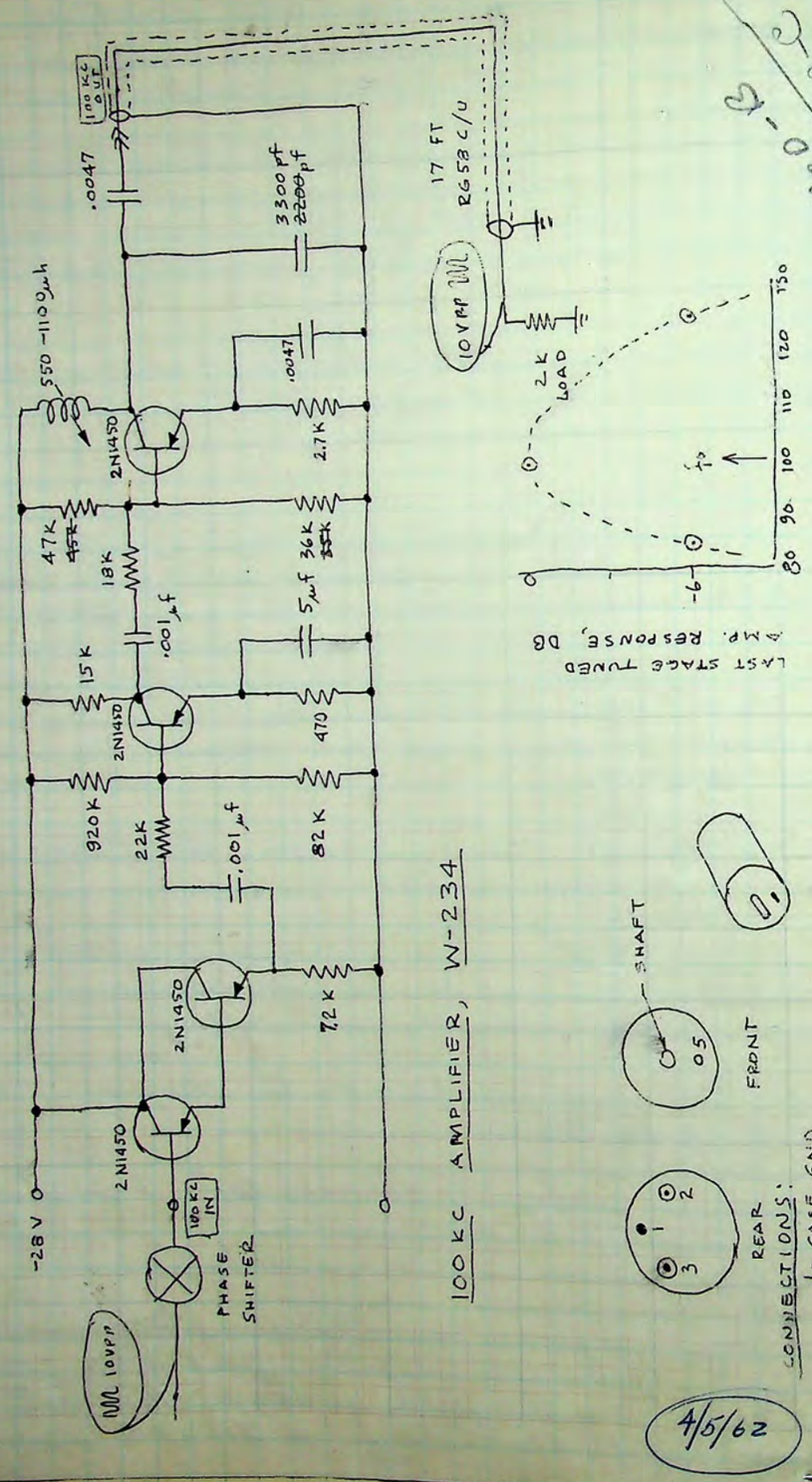
Letters sent to various transistor circuit module manufactors for info on possible applicable circuit packages for the FPN-38 reset circuitry —

Ordered rack for holding the equipment of the FPN-38 project (4/4/62):

Received info from 3CGD(f) that φ shifter package from NILSEN has been ordered

4-8-62: The trigger waveform generator originally built has an objectionable negative spike when button is released - this could re trigger the gate-FF and disrupt the reset logic - therefore investigating

100KC AMPLIFIER (FOR USE W/ Φ SHIFTER)



100 KC AMPLIFIER, W-234

4/5/62

W-234 (CONT).

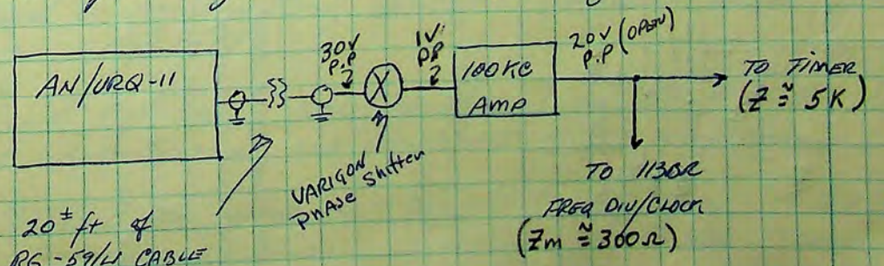
4-8-62 (CONT)

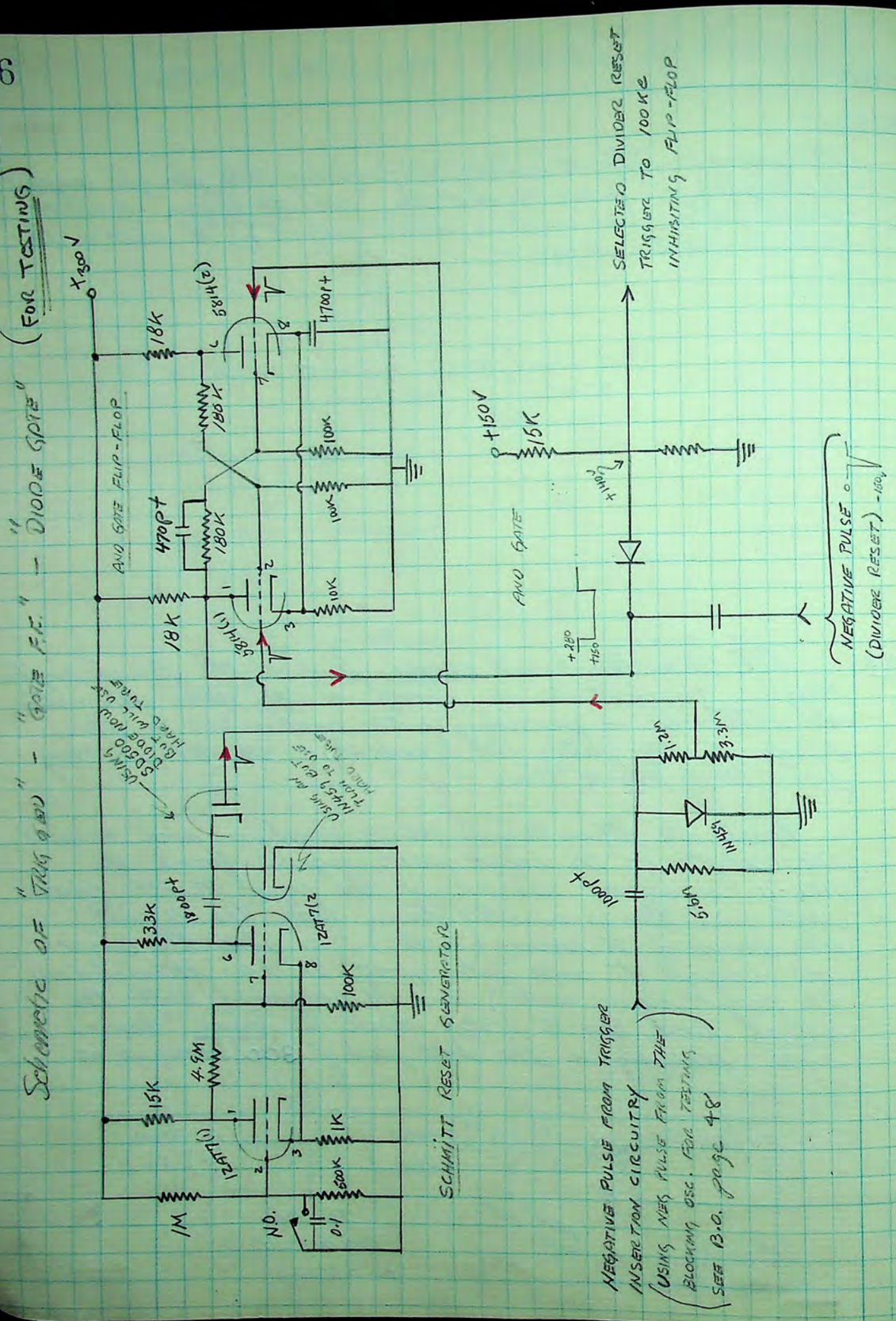
the use of a different method of producing the desired negative reset pulse - breadboarded the "schmitt trigger" circuit shown below (as used in decca project) to obtain the desired negative trigger -

(See NEXT PAGE - SCHMITT TRIGGER GEN.)

4-9-62 Tests show this circuit should produce the desired negative trigger - amplitudes as shown on the above schematic are obtained - proceeding with application of this trigger to the gating-F.F. (see p. 47) - this F.F. is copy from the AN/FPN-41 timer -

Tested the transistorized 100KC amplifier and varigon phase shifter - the input 100KC signal from the URQ-11 is approx 20V-P.P. at the input to the phase shifter and this is a little larger than the circuit was designed to receive (10-15V) - also the amp was designed to work into about 2K (as stipulated in the project requirements) and it was found that the actual load due to 113BR clock is much lower and probably in the ball park of 300 ohms or so:





W-234 (cont)

4/8/62 (cont):

The result of the poor impedance match between amp and clock was a marked decrease in amp output and a lot of signal distortion — since the clock will work on 100KC signals down to 1/2V-p.p, plan now to put a large resistance voltage divider on the amplifier output to the clock to achieve desired match — use of ~~emm~~ emitter follower @ 50Ω abandoned due to large current drain — ie limited by using HP-724 power supply —

Tests with ~~trigger~~ "gate flip-flop" using the push button trigger and the negative trigger from the blocking oscillator are encouraging — now need to balance out the triggers and get them in the ball park amplitude of the divider used — F.F. output is approx 100 VOLTS — increased this to approx 150V — now proceeding to test the gate.

Modified the 100KC solid-state amplifier with a large R voltage divider output and also changed bias levels — now can get about 15V-P.P. output out of the amplifier going to timer (open circuit) and about 2 VOLTS to drive the HP-113-BR clock (should be enough) — ie req are min of 0.5V-rms (or ~1.5V p.p.) — thus the amp sees a relatively large impedance working into clock & open circuited to timer — since the AN/FPN-41, 100KC input impedance is ~5K, there should be no adverse loading on the amp when the timer is connected — the amp. is being re-wired to include the voltage divider and an additional BNC connector — this will then be re-tested and with timer load connected —

4/10/62:

Moving the trigger generation set up to alternate bench location so can allow decca project work in this area on receiver —

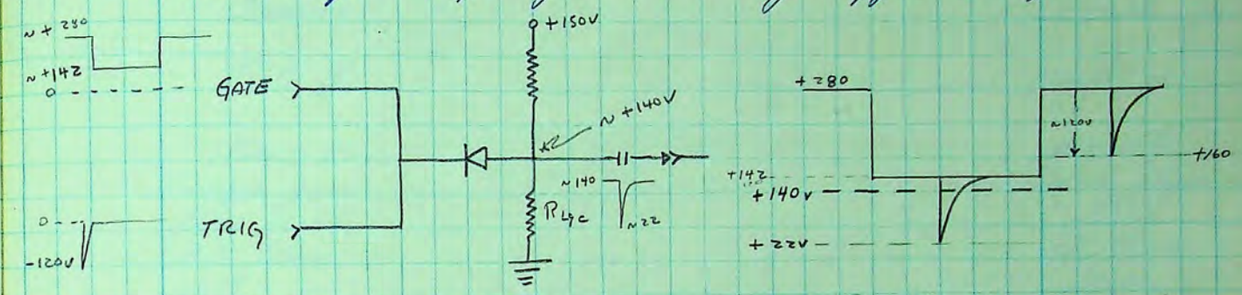
Send HP-160B oscillascope, serial "A", to lab for general maintenance and check out of preamplifier, etc —

Continuing to work on the 100KC amplifier — the low clock input impedance causing loading problems — may have to go to a larger output transistor — circuit is

4/10/62 (CONT) presently adjusted to provide 2V-P.P. to the clock and about 15V P.P. open circuit across the voltage divider (ie where timer load will eventually connect) — letting this run now to see if we are pushing the circuit transistors too hard —

LEGAL WORK TODAY

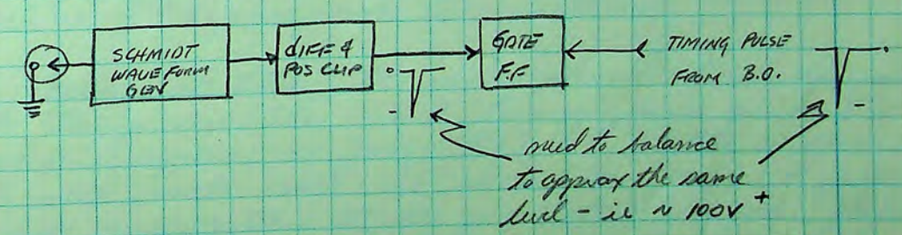
Continuing on with adjusting the trigger circuit F.F. output to gate & bias on diode in gate to get max trigger thru the gate (hope to get ≈ 100V neg trigger thru gate):



ie, negative trigger alone should not get thru the gate or should gate alone but trigger + gate should get thru OK to give approx 100+ VOLT neg trigger out. - (ie AND GATE)

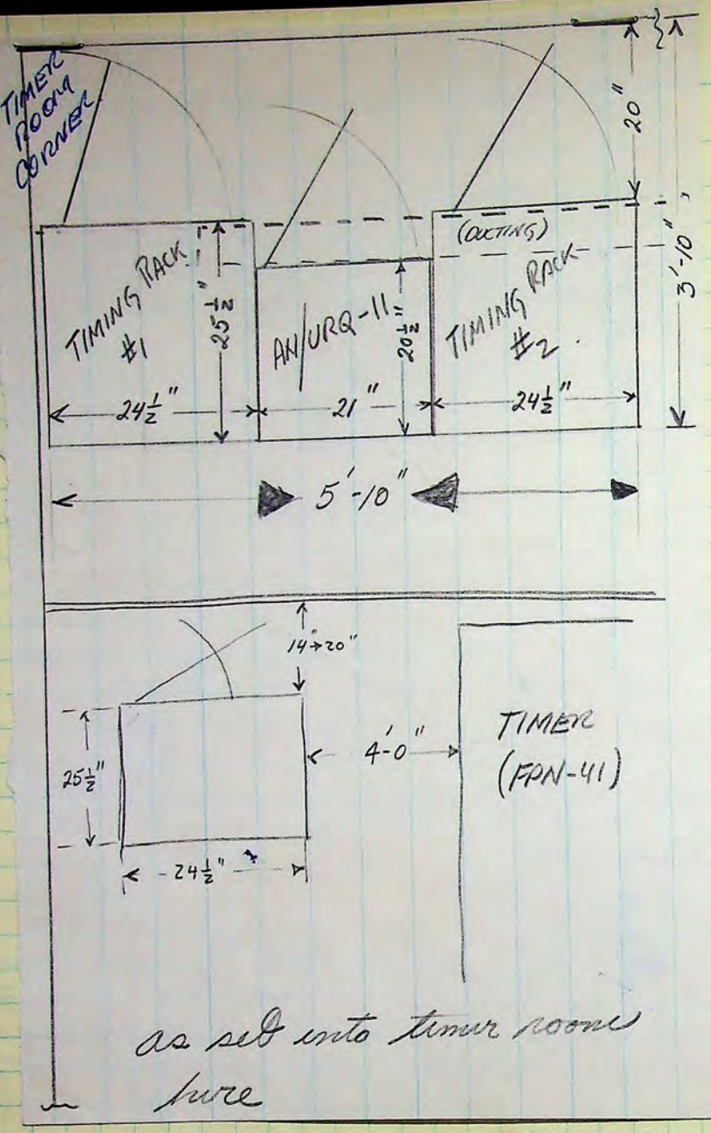
4/11/62: Working on balancing signals from schmidt waveform generator to the gate flip flops to match the negative timing trigger from the blocking oscillator in order to have the waveform flip-flop operate as desired (see waveform above) —

LEGAL WORK TODAY ALSO



Set the diode gate levels and it appears that the levels shown on above sketch can be obtained and will allow for proper gate operation:

Continuing with sonic amplifier — operated all nite and clock operation appears normal — the output transistor is a little warm so now investigating a little higher power output transistor —



as set into timer room here

W-234 (CONT)

4/11/62 (CONT)

Continuing with testing & refinement of the reset circuitry — the 100KC amp still operating satisfactorily.

4/12/62: Continuing with reset circuit — have stable operating circuit up to & including the gate — plan now to refine the breadboard set up and move into timer room to test gate using the divider reset —

Commenced installing new equip rack in timer room —

Note to LCDR Edwards on screen room dimensions —

Have cleaned up the breadboard of the reset schmidt trigger generator, blocking oscillator, gating waveform flip-flop and the diode gate — now ready to take into timer & check how divider reset will get thru gate — timer will be tied up the first 3 days of next week so this will have to be done after that:

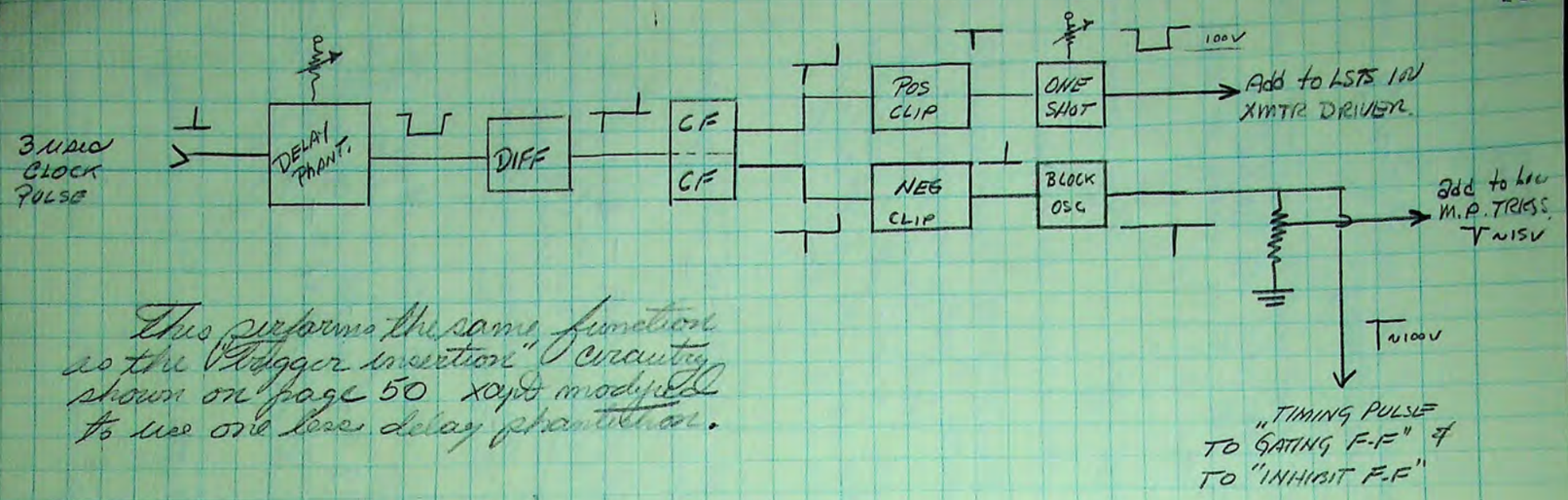
4/13/62: Continuing with setting up the AN/FPN-41 timing rack in the timer room with HP equipment —

HP-160B scope #A returned from lab — has been checked & aligned — have ordered a P-7 phosphor tube + filter to check operation in scope for the one PPS operation — found that scopes as sent have a P-1 phosphor tube installed —

Commenced testing the delay phantastron designed for the trigger insertion and timing pulse generator (see block diagram on page 50) — sketch of circuit as it will work will be shown on p 51 — performing minor modifications to the phantastron as per "preferred circuit" hand book —

4/16/62 Continuing with delay phantastron circuit and modification to achieve desired waveforms

Continuing with setting up equipment rack in timer room



This performs the same function as the "Trigger insertion" circuitry shown on page 50 xcept modified to use one less delay phantistor.

TYPICAL DATA ON DELAY PHANTESTRON (NEXT PAGE):

Basic consideration: as R_1 is decreased (lower voltage on center tap) the rise and decay time of the pos & neg pulse resp decreases as well as does the pulse amplitude. Increasing the control voltage (& thus lengthening out the delay) increases the rise time with an increase in pulse amplitude —

RUN #	RANGE OF DELAY	R_{1A}	R_{1B}	R_2	E_{CONT}	DELAY (μsec)	t_R (NEG PULSE)	t_R (POS PULSE)	REMARKS
1.	440-1320	8.3K	14K	2.4M	—	1000	5 μsec (120V)	7 μsec (100V)	RISE TIMES TOO LONG
2.	1000 →	~22K	0	4.4M	(LOWER)	1000	2.8 μsec (75V)	3 μsec (60V)	NOT ENOUGH RANGE BELOW 1000 μs delay
3.	800-2600	~22K	0	3.7M	+92V	800	2.5 μsec (80V)	2.5 μsec (60V)	approx optimum conditions — will adj for range 800-1200 μsec — (t_R-OK)
4	800-2600	~17K	~5K	3.7M	+114V	1200	3.0 μsec (100V)	4.0 μsec (75V)	

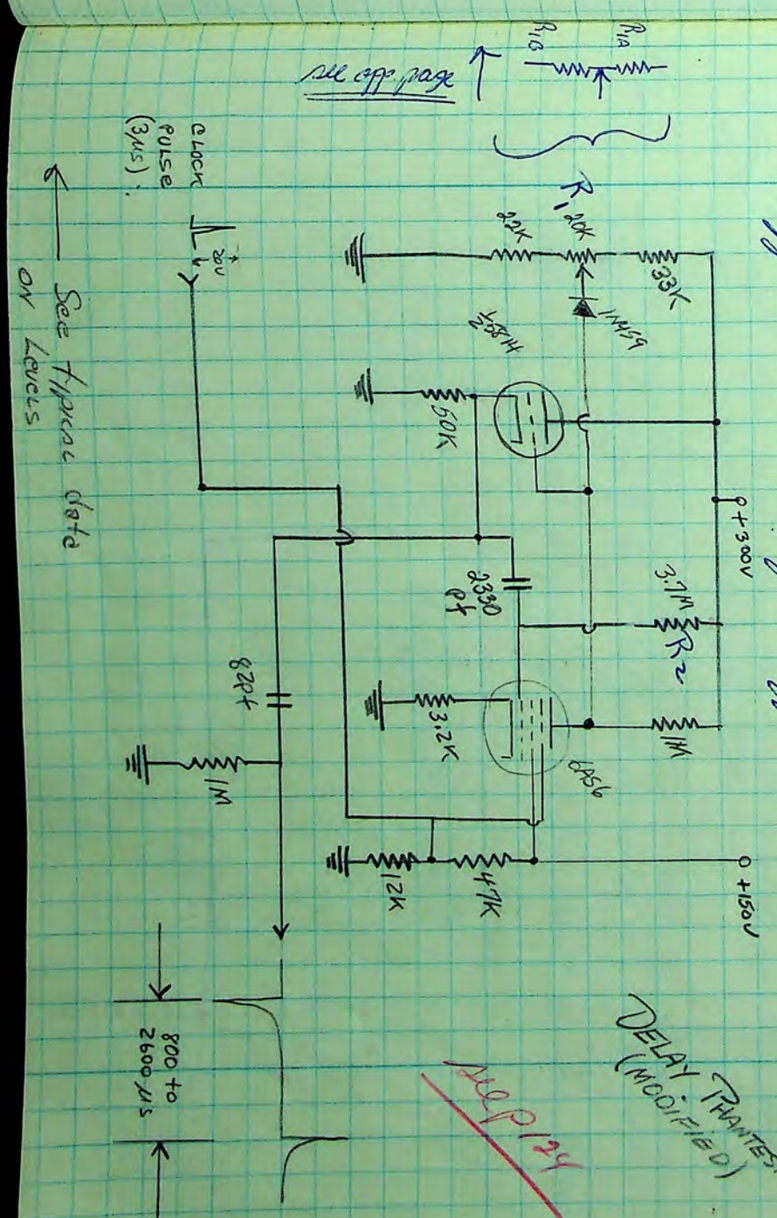
W-234 (cont):

4/17/62 — completed basic timing card installation in time room including in rack in hp-160 scope, hp-time computer, hp-clock (1μs), the monitor patch panel blank and the trigger selector panel blank + 200c bright & RS - 4 cable from output of the above amplifier (operating on 100V) to point of 100V amp operating - clockpulse FPM-41 above channel chassis: - 100V amp operating - clockpulse.

Continuing on with delay phantistron operating on the clock (+) pulse to give timing pulse — see schematic page (62) for property proposal. Block diagram —

4/18/62 Work on proceeds ~ 3 watts (p.p) to clock & input 13 +15V (p.p) to time (slow long run of coax connected to J-1 in 100VCC channel chassis) - this is lower than 20V (p.p) designated to provide input to the time left time above input of — going block to design more power out of 100V amp on timing rack — providing for ~ 20V p.p at the time input J1

Continuing with phantistron circuitry — here comes up with below modified delay phantistron gives detail trigger as shown (after differentiation):

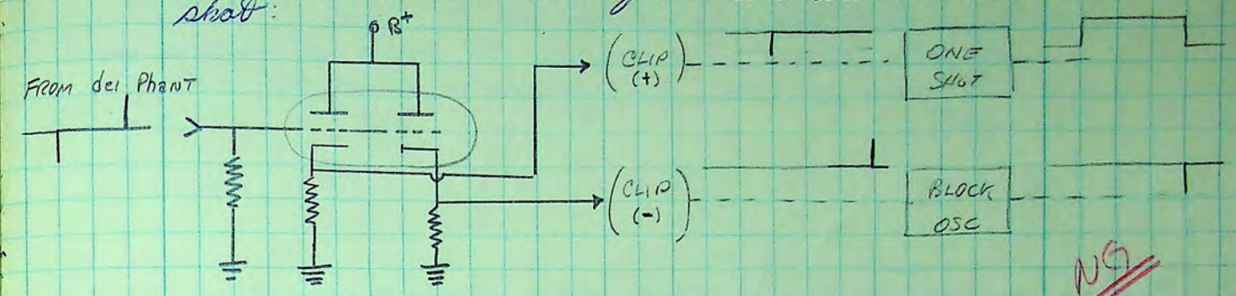


DELAY PHANTESTRON (MODIFIED)

see p 129

W-234 (CONT):

4/19/62 (CONT): Proceeding to operate on delay phantastron outputs — plan to feed signals thru a double cathode follower before clipping and then on to the blocking osc and the 1000 usec one shot:



C.F.

NG

Going back to reconsider placement of the various component sections of the system — due to relatively high power already being drawn from the LAMBDA power supplies at the breadboard, we may need one LAMBDA for each set up to avoid overloading the tower power supplies —

It may be wise to install the timing pulse, trigger generation and LSTS generation circuitry in the timing control cabinet and then only have the resto circuitry in the XMTR dem drawer. — will decide after tests —

4/19/62: 100KC amp still operating properly — clock operation normal on voltage divided output — output transistor is slightly warm —

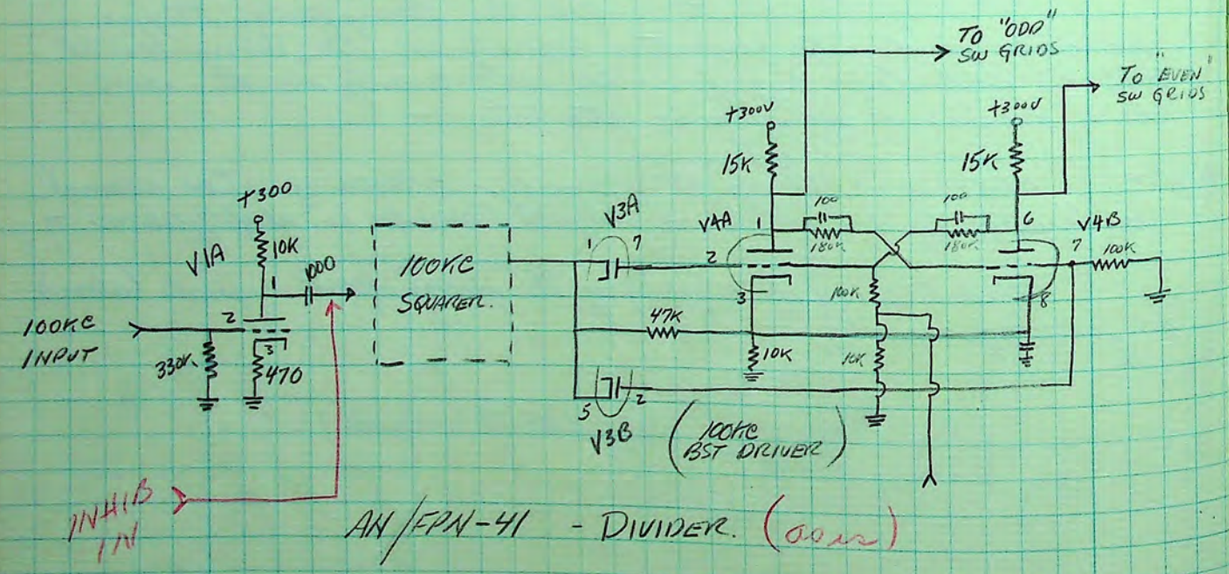
Achieved adequate clipping of the delay phant signals (above) in following manner —

(CLIPPERS ON delay phant output)
include C.F.

NG

100KC - BST:

Blank is formed on spade (target) nine (9) by the negative pulse of divider reset —
Divider reset also goes to the 100KC BST-Driver and hits the grid of V4A causing the half of the F.F. to turn off.



AN/FPN-41 - DIVIDER. (00 ss)

10-234 (CONT)

4/19/62 (CONT): applied positive (delayed) trigger to the blocking oscillator (see p 48) in following manner with pulse as shown:

(trigger to B.O. & output/input data)

see main schematic

Commencing application of the negative pulse to the "1000 usec one shot" M.V. (see circuit on page 24) to form the "LSTS add" waveform:

(neg pulse to one shot)

see main schematic

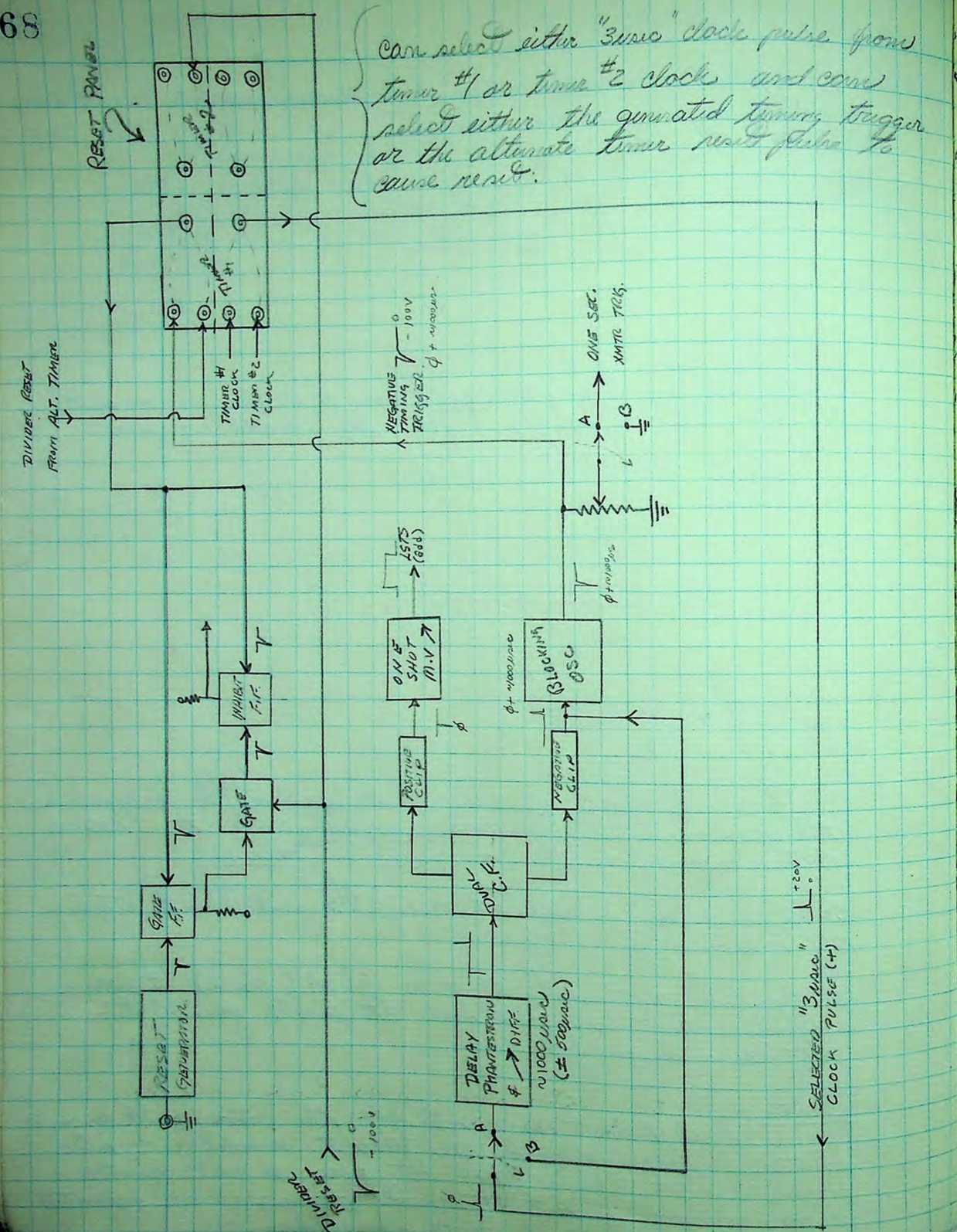
Performed meas. of voltage levels needed to be applied to various sections of 100KC signal path to 100KC BST driver in divider — results as follows:

① Applied neg 20 volts to grid of V1A and able to stop BST action

② Applied +100 volts to grid of V3A (pin 2) to achieve desired inhibit or -100 volts to pin 7 on V3B to get desired inhibit.

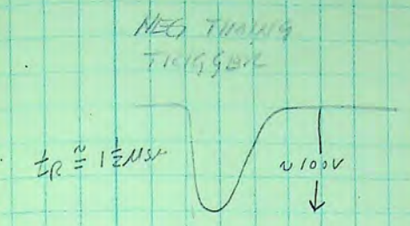
RESULTS: Will have to wait until get the entire resets circuit installed before deciding on how to inhibit — also will have to assure that BST does not switch upon inhibit due to transients — waveform generated by F.F. to be ± 100 VOLTS minimum —

can select either "3usec" clock pulse from timer #1 or timer #2 clock and can select either the generated timing trigger or the alternate timer reset pulse to cause reset.



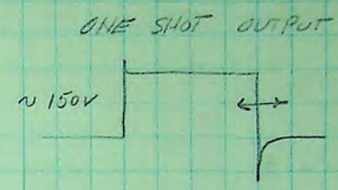
W-234

4-20-62: Continuing with cleaning up the waveforms and negative trigger being generated by the "one shot" and the "blocking oscillator"



PULSE WIDTH ≅ 5 usec

this seems ok — will decide down to ~15V for the one second transmitter trigger and use full amplitude for the timing trigger!



P.W & t_R are ok — must get rid of leading & trailing transient — negative return of grid (see p.24) is probably the trouble on the trailing edge

Received phone call from LT BAETSEN on the project — target date for completion is to be moved ahead to 1 August 1962 for the FPN-41 and to 1 September 1962 for the FPN-38 — this to come down in writing —

Opposite page block diagram shows entire reset/trigger insertion systems as presently being built and shows how system applicable to all Lavant rates plus how the alternate timer information is used to reset the timers —

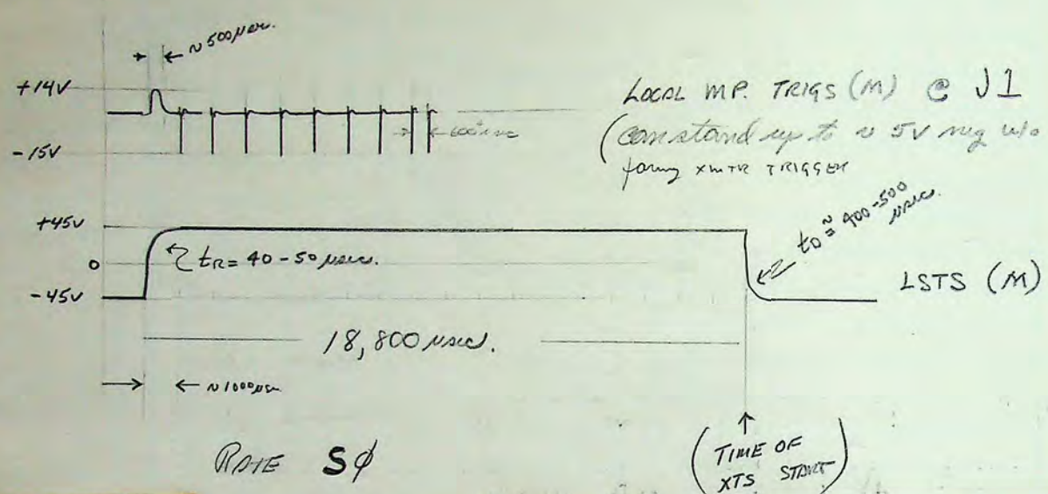
SWITCH POSIT "A": In this position the "one second" transmitter trigger is generated and "LSTS-add" is generated to allow proper transmission of the one second timing pulse. — negative timing trigger is generated.

SWITCH POSIT "B": In this position the "one second" trigger and "LSTS-add" are not generated and only the negative timing trigger is generated and fed to the "reset panel" — The "3usec clock pulse" is fed directly to the blocking oscillator and thus the timing trigger is formed at time Φ with respect to the clock pulse —

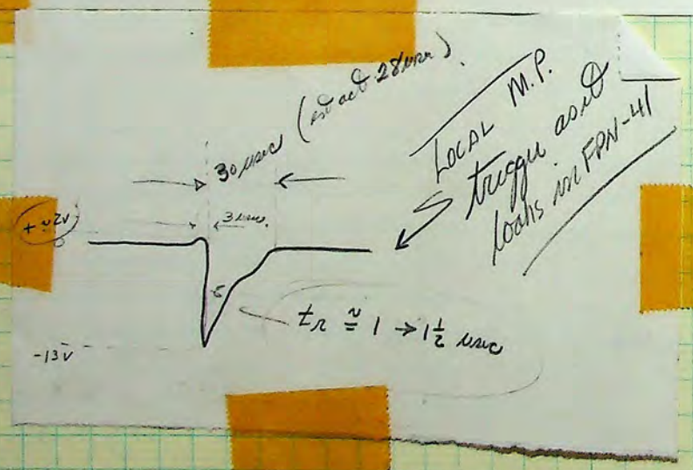
Repeated mods of "XMTR DRIVER" waveforms.

XMTR DRIVER WAVEFORMS
AN/FPN-41

18.
9.4
2000
18.8000



RATE S0



Waveforms that we must match for one second trigger insertion and the addition to LSTS.

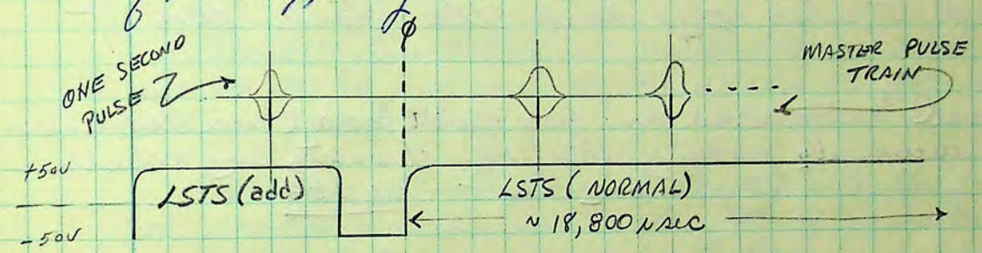
W-234

4/23/62: Continuing with cleaning up of the "LSTS-add" waveform out of the one-shot-M.V. (eliminating negative spike on trailing edge

Mr Shujiro working on the "reset circuitry" for use in FPN-38 part of the project — rough schematic has been worked up using complete transistor circuits — transistors have been ordered —

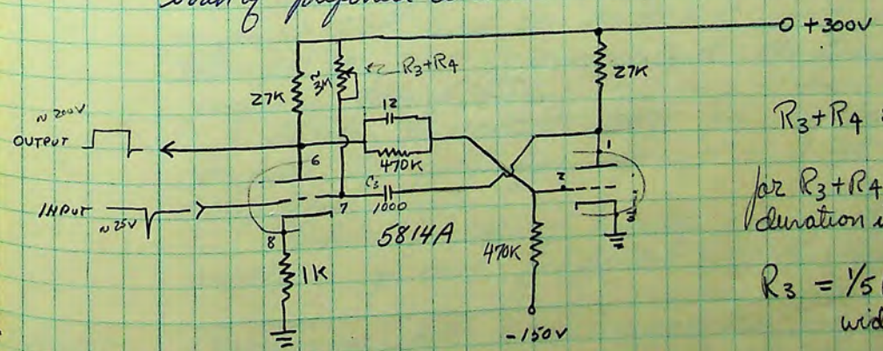
Remember XMTR driver waveforms in FPN-41 — LSTS add must be long enough to properly gate out sufficient 100KC and start early enough so that the chopper in the sweep will drive in time

∴ it must start about 1000 usec ahead of the one second trigger and it must extend out past the time of the trigger by about 300 to 500 usec



Also must operate on the "one shot-M.V" output to get 100 VOLT pulse ±50 around V=0 as is normal LSTS —

Having difficulty getting clean one shot output pulse with circuit of page 24 — trying one-shot circuit from handbook of published circuits



R_3+R_4 : 550K → 3M

for R_3+R_4 = 2M, C_3 in pf = gate duration in μsec

$R_3 = \frac{1}{5}(R_3+R_4)$ for ease in gate width adj

(see p. 41-2 of NAVAER 16-1-519)

5/10/62: Check of HO-7/113BR divider/clock ser # 11000175 at Rad Wash — triggered scope from 113AR clock ser No 01300123 and observed a jump (delay) of 0.9 usec in the 1KC triggers when switched to 1KC meter position (ie jump in 113BR triggers) —

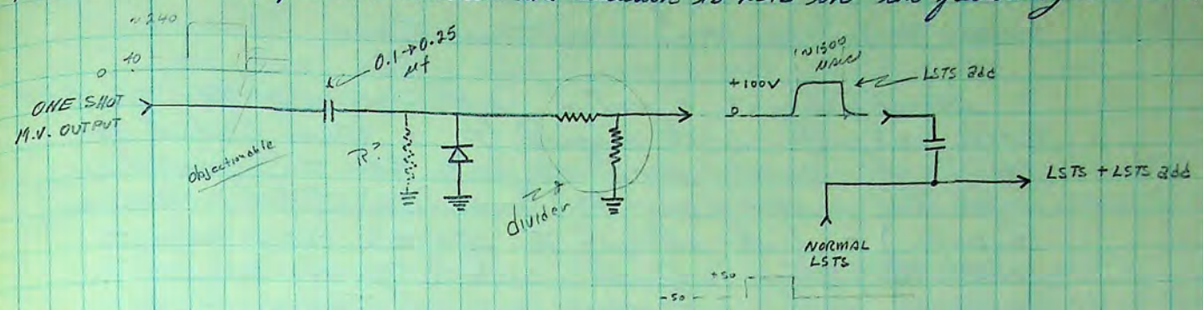
Then switched 113AR clock to 1KC meter position and observed a 0.2 usec jump in that clock —

Hewlett Packard Co rep in Wash area contacted by HQ (Bartsen) and Rad Wash (Mizell) — they are going back to Palo Alto for info and will advise when they check their clock there —

5/31/62 Received "recommended fix" from Hewlett Packard via Radio Wash and successfully modified both clocks eliminating any noticable pulse jump in 1KC position of sw — see p 84

W-234

4-23-62 (cont) Propose to add in the addition to LSTS in the following manner:



4-24-62: Continuing to clean up the negative spike on the trailing edge of LSTS-add. Changed pot in one-shot to give range of this waveform from 1000 to 2000 usec

Phone call from LT Bartsen: project dates moved to 15 July '62 for the FPN-41 part and 15 Aug '62 for the FPN-38 part — letter to follow:

Planning to get the reset circuitry into the timer room as soon as possible while the FPN-41 is not obligated and to make necessary circuit changes as soon as possible so that parts ordering may be done asap & before 18 May (as per station notice No 13-62) —

4-25-62 Commencing to clean up all the various circuits already fabricated (all the trigger insertion sections plus all the used circuitry except the 100KC inhibit flip-flop) and mounting on one rotor board. These will be given a final test and the last F.F. will be constructed — Then all this will be moved into the timer room so can perform desired tests: —

Starting to collect data for needed parts ordering to complete the proto type set up and to build the completed units

Making sketches of circuits & indicating operating voltages as clean up and rebuild (see π (above) —

4/26/62: Continuing with same work as on 4/25/62 — drawing up complete schematic of all circuits:

W-234 (CONT):

4/27/62: Continuing to clean up breadboarded circuit for testing reset/trigger insertion circuits in timer

Investigating a reported shift in time of the HP-113BR clock outputs with respect to a timer locked on the same 100 KC osc on rate 5Φ - (reported in informal note from CO Loran XMTG station, Carolina Beach) - first attempt to compare clock outputs with ~~the~~ timer-divider used (FPN-41) on rate 5Φ showed drift but drift reduced to zero by de-activating the 100KC envelope servo drive ? (Debrues on note & can cause errors) - observed a 0.2 usec shift in timing (instantaneous) when shift to 1KC meter position - checked out clock and found voltages on Q-6 different than listed in manual for the gear (see below):

Measurements on "Q-6" in HP-113BR DIVIDER/CLOCK:

	DIVIDER ON CLOCK RUNNING		DIVIDER OFF	
(VOLTAGES)	(AS PER BOOK)	(ACTUAL)	(AS PER BOOK)	(ACTUAL)
EMITTER:	-1.4 VOLTS	-1.19 VOLTS	-0.410 VOLTS	-0.460 VOLTS
BASE:	+0.6 "	+0.16V	-0.020 "	-0.04 "
COLLECTOR:	-11.9 "	-12.1V	-11.9 "	-12.1 "

took same meas w/meter switch in 1KC position:

	-1.1 VOLTS		-0.405 VOLTS
	+0.22 "		-0.04 "
	-12.1 "		-12.1 "
Δ Emitter:	+0.09 VOLTS		+0.055 VOLTS
Δ Base:	+0.06 "		Φ
Δ Collector:	Φ		Φ

note that get significant change in emitter voltage at no signal conditions -

Meter Readings on front panel

SUPPLY: 6.5 (6.5) 10KC: 8.1 (7) CLOCK: 7.0 (8.5)
100KC: 6.9 (7) 1KC 9.1 (7)

W-234 (CONT)

4/30/62: Have cleaned up the breadboarded reset/trigger insertion circuitry and now setting up on card with power supplies for final testing before moving into timer room for operational tests:

SENT 4/30/62 → Preparing note to CO Loran Carolina Beach telling of results on clock shift and readings taken in the clock circuits -

Send HP-160B scope (#B) to lab for installation of P-7 CRT and check out of pre-amps - oiled both clock A & B in accordance with instr. manual -

5/1/62: Continuing to clean up & de-bug breadboard reset/trigger insertion circuitry:

TAC meeting (3hrs) - preparing annual Farewell Day literature and civilian personnel job descriptions

HP-160B scope (#B) returned from lab - initial tests show definite increase in slow psn pulse resolution - will have to test using our signals now to be sure -

5/2/62: Continuing to de-bug breadboard -

found 6W4-GT tubes (2ea) in lieu of correct 6U6-GT tubes (2ea) in LAMBDA power supply - found they had been inadvertently inserted by tech earlier and not due to theft.

Writing job description for Civilian Employees - setting up Annual Farewell Day - scope procurement discussion - SKUJINS assisting on project.

5/3/62 Wired reset/trigger insertion circuitry into FPN-41 timer room to commence initial tests - bringing attenuated divider reset into the reset gate and then will form 100KC inhibit to determine just where we want to apply it in the 100KC channel chassis -

Having difficulty with the "divider used" gate -

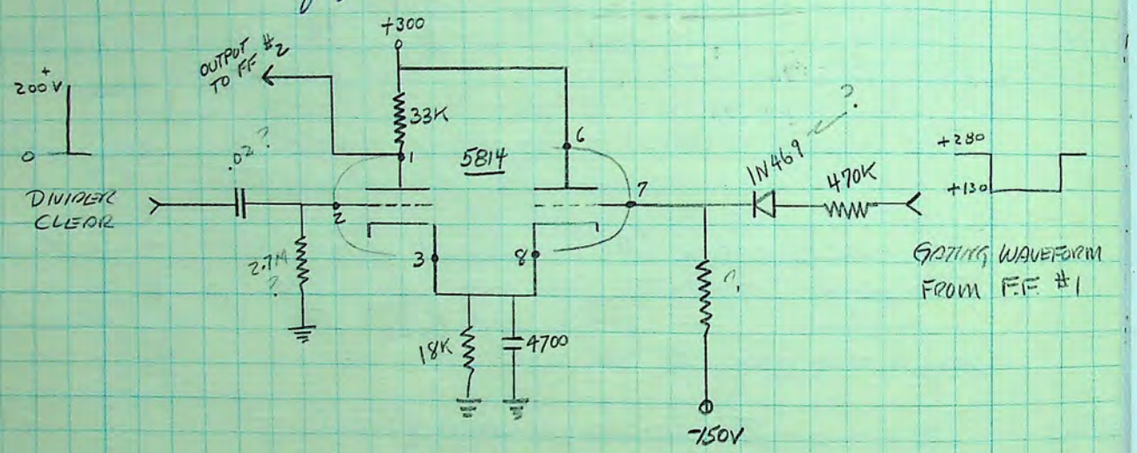
Timer obligated for East Coast Chain op - SECURED

W-234 (cont'd)

5/3/62 → 5/9/62: Priority use of FPN-41 timer on other projects precluded any significant progress – work being done on design of more suitable gate for divider unit and gate for adding in the LSTS addition

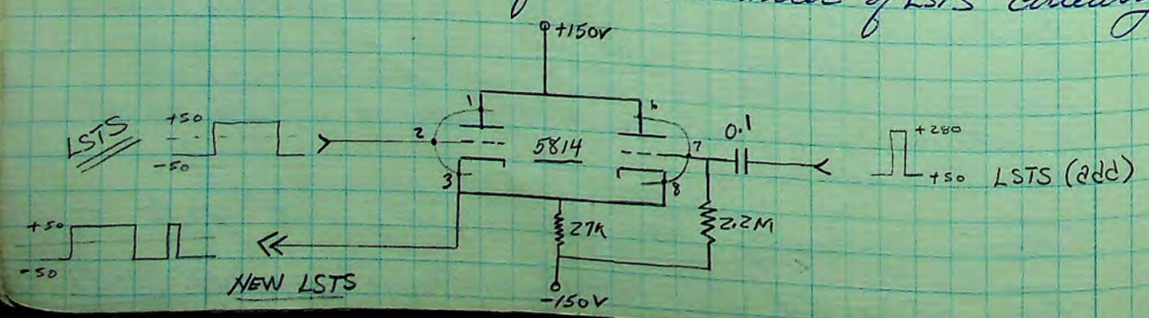
5/10/62: Constructed reset/clear gate and commenced tests:

5/11/62: Completed tests on divider clear gate (in lieu of divider reset as previously attempted) – Rough schematic of gate as below:



5/14/62: Trouble with 100KC osc (URQ-11) in AM and worked on that –

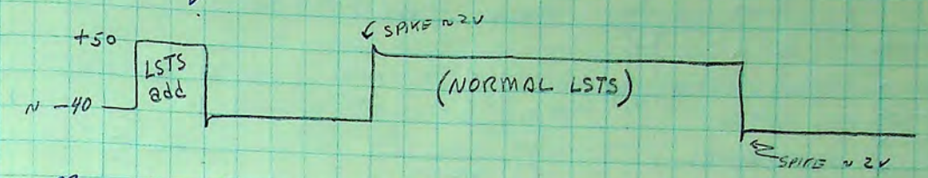
Commenced working on LSTS add insertion – approach to problem is to add normal LSTS and LSTS add on opposite grids of a dual triode taking outputs off common cathode resistor – this should give desired isolation from remainder of LSTS circuitry –



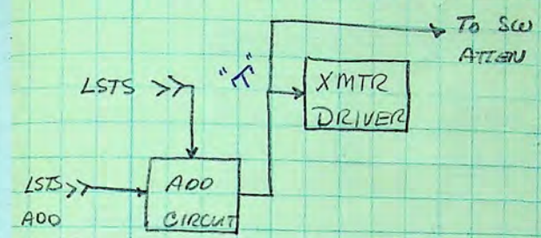
W-234 (CONT)

5/14/62 (CONT).

Tests of LSTS insertion circuitry successful – below waveform is resultant product:



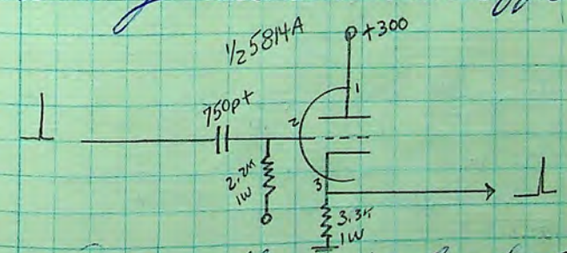
Now will have to test on timer by adding on XMTR drawer:



No feedback of LSTS add observed – get complete isolation

5/15/62: Working on running "divider clear" from the divider drawer thru length of RG-59/BU cable (75') – considerable ringing experienced – difficulty running thru open wire due pick up and poor impedance matching giving a NEG pulse on grid of gate –

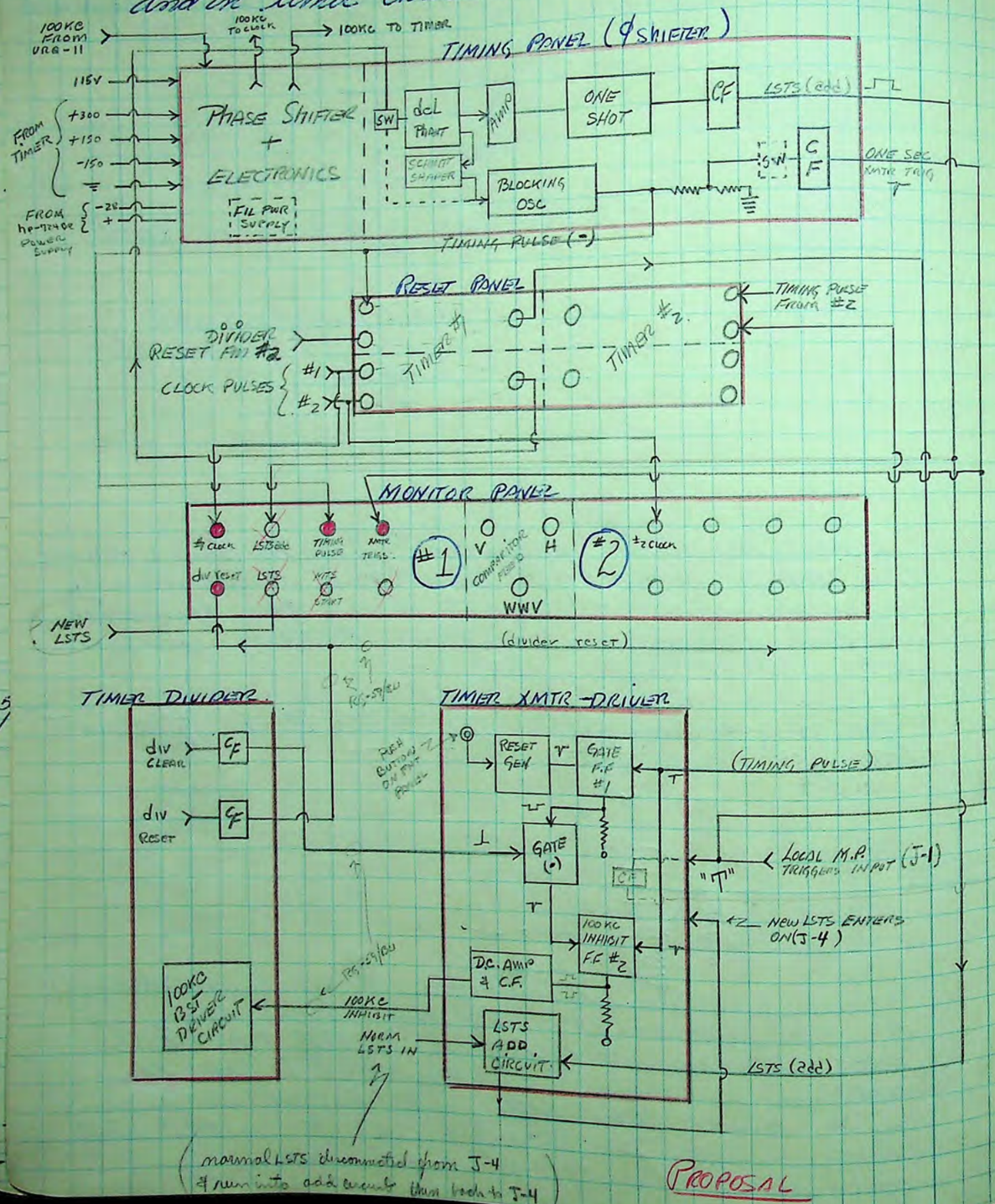
Building cathode follower for divider clear to alleviate loading and distortion effects –



successfully ran divider clear from divider drawer to test stand (12-15' RG-59/BU cable) using C.F. – Put clear signal on grid of F.F. #2 and achieved successful switching of F.F. on the first divider clear after reset button is pushed with subsequent flipping back to initial state upon receipt of my one second timing pulse –

W-234 (CONT)

5/15/62: Present plans for equipment layout: in timing cabinet, and on timer chassis:



W-234

5-16-61: Commenced operating on the F.F. #2 output waveform in the attempt to restore the high dC level (+) & (-) going inhibit waveforms to a zero level so have 0 → +100 and 0 → -100 valt waveforms resp — various approaches tried w/o success — must dC couple the waveforms, so do not loose signal due to slow rep rate (may one second pulse) — also must not disturb the FF #2 action —

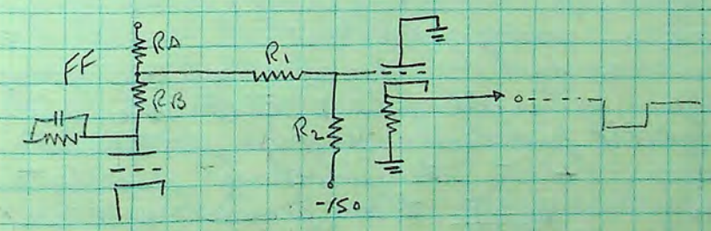
Also started working on ordering of ~~[illegible]~~ parts for the timing circuitry —

Worked on AF day preparations —

5/17/62 Continuing on work to achieve desired waveform coupling from 100KC inhibit F.F. — approaching problem from the DC amplifier aspect now —

Received phase shifter packages from NILSEN MFG Co today —

5/18/62: It appears dC amplifier arrangement will work on the inhibit waveform to bring the quiescent level down to zero volts d.c.



$R_A + R_B$ = normal plate loadon F.F. : division of R_A & R_B to be determined such that waveform amplitude picked off is small enough to allow minimum R_1/R_2 voltage division and large enough so size of R_1/R_2 will adiquately isolate F.F. from the dC amplifier — ie too large R_1 & R_2 will introduce significant RC time constants with small C's already present causing distortion of leading & trailing edges of the inhibit waveforms — too much of this cannot be tolerated if expect to achieve divider cut off as needed w/o delays —

W-234 (CONT):

5/18/62 (CONT) P.M. no progress – setup torn down to make way for AFD displays

5/21/62 – Better part of AM spent on showing AFD set up to visitors – proceeding to re-set up the timing circuitry and to continue on with 100 nc inhibit waveform problems –

All basic ordering of parts (incl. B.O. xfmr and two filament xfmrs) for second setup and for re-doing pulse set-up, have been ordered (done on 5/18 and 5/21)

HP-160 scope (unit A) sent to lab for repairs – would not come on when turned on

Rest of day spent re-setting up equipment and investigation of reason for malfunctions

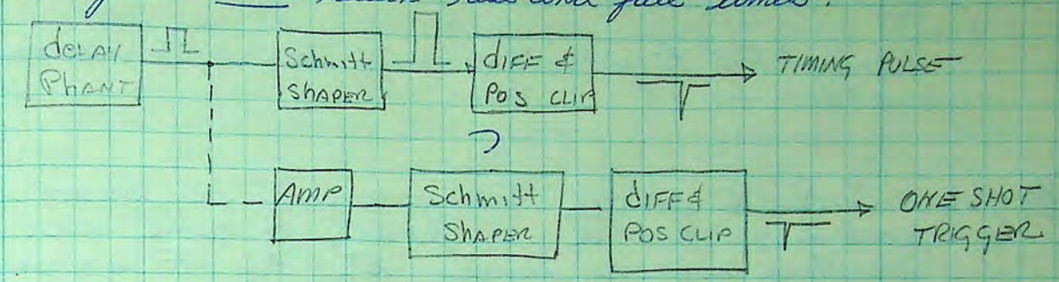
5/22/62: Continuing to re-set up timing breadboard – all circuits in operation as before by 1630

5/23/62: Need to clean up the timing (neg) pulse – going back as far as delay phantastron circuit to see why pulse so bad – found that in going thru amplifier after del phant that the rise and fall times of the pulse are badly perturbated giving a pulse (+) to the blocking oscillator with a rise time greater than 5 usec and a width of from 20 to 30 usec – this is completly unacceptable – unable to improve the wave shapes changing components to reduce RC time constants –

W-234 (CONT)

5/23/62 (CONT):

Now investigating possibility of using a SCHMITT SHAPER on the delay phantastron output in order to raise the level of the waveform and retain rise and fall times:

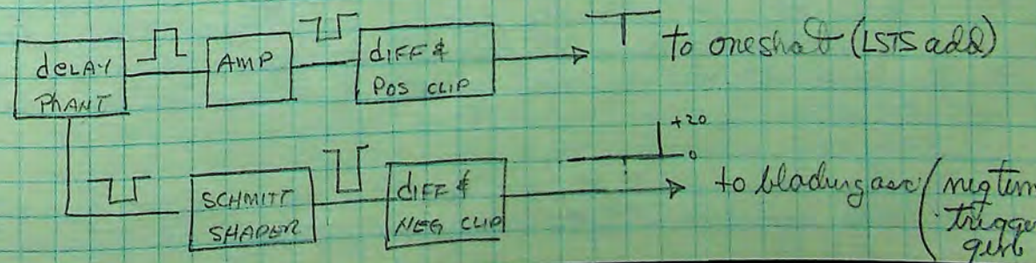


This would eliminate need for the blocking oscillator and give us a solid negative timing pulse (and XMTR trigger) for F.F. operation.

Then propose trying amplifier on to delay phantastron output to get inversion & then thru Schmitt shaper (if necessary) to get some gain (may not be necessary) – since timing of LSTS add waveform is not as critical as the neg timing pulse – such sophistication may not be necessary –

5/24/62 Continuing on with ideas on shaper (above) – build a Schmitt Shaper and attempted to drive with a positive pulse – unable to drive the circuit hard enough (due grid limiting action & cathode feed back loop) using positive input –

Then took negative delay phant waveform from cathode and successfully applied this to the shaper to get a good (1 usec or less) rise and decay time on the output wave shape –

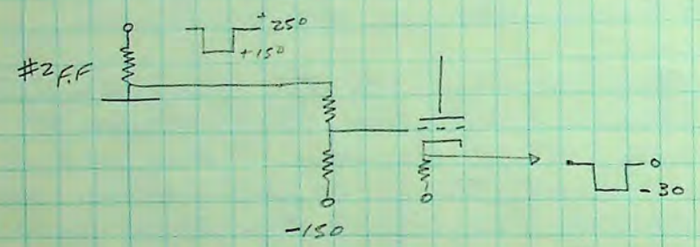


5/24/62 (CONT)

differentiated and negative clipped the shaper output to get a good positive trigger to the blocking oscillator (~ 20 volt amplitude) — output trigger from B.O. now looks much better —

Worked PM to get all circuitry back into normal operation —

5/25/62: Cont. to get all timing circuitry on bread board working as desired — finally succeeded and resumed work on bringing the #2 FF waveform down to a dc level which can be used to inhibit the 100KC BST circuitry —



used (0 → -30) or (0 → +100) volt waveform to achieve desired inhibit of divider.

100KC amplifier (new) built and installed with clock / timer input using output 100KC from the VARISYN of skylab — operation seems normal with minimum of 100KC distortion

PARTS PARTIAL arrived for timing circuitry arrived today —

5/28/62: Cont. to get inhibit waveform leads — plagued with #1 F.F. problems — circuitry not working correctly — trouble shooting — corrected problem in #1 F.F. put small commutating capacitors across both plate to grid resistors and circuit appears to be oper. O.K.

Now commencing to fabricate a circuit for operating on the inhibit FF #2 waveform (+ going on inhibit) thru

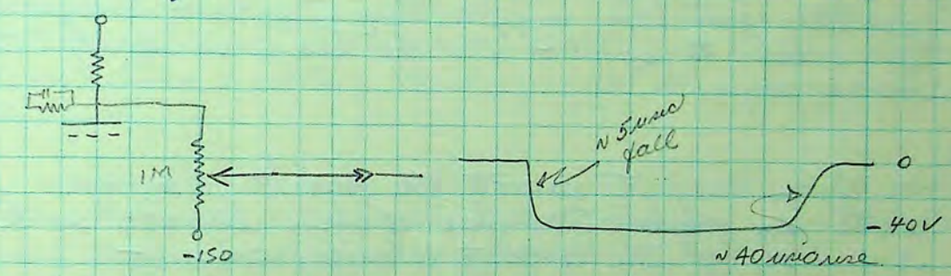
5/28/62 (CONT):

a dc amplifier (dual stage w/second stage a CF) in the attempt to get an inhibit waveform going from 0 to negative 30 volts or so —

5/29/62 Hooking up the above described circuit into timing bread board —

Could not get a dc amplifier arrangement to work properly to bring the inhibit waveform down to the desired level — in order to get satisfactory levels into the dc amp tube, the voltage divider necessary (large R) and the tube action caused unacceptable delays in the rise and fall of the inhibit pulse

Went back to a simple voltage divider across the inhibit F.F. output (1M pot centertapped output with the low leg to -150)



Due to the large voltage divider values, the inhibit waveform rise and fall went out 3X or more than when meas. directly off F.F. plates —

Inserted the above waveform onto the grid of the 100KC amplifier in the divider and achieved a consistent reset except that the divider reset produced on successive intervals after manual reset were displaced (delayed) by about 300 usec — this was consistent though not a desirable reset.

The problem may be due to several factors:

① The delay in time of "un-inhibit" with respect to the time of negative reset pulse (ie large positive rise time) may be uninhibiting the 100KC amplifier too late

② The 100KC squarer may not be getting back into

W-234 (CONT)

5/24/62 (CONT)

proper operation fast enough - if either it or the 100KC amp may be getting "shocked"

The important thing is that the timing waveforms appear to be OK in the reset circuitry tried breadboarded and the principle of this reset should work out OK

Intend now to do the following

① Attempt to reduce the resistive voltage divider values to get a desirable inhibit waveform w/o so much Resistance to give rise to large RC time constants w/ the tube, etc

② Attempt to get more amplitude either from the positive going or negative going inhibit waveform in order to inhibit the BST drive in lieu of the 100KC amp.

5/31/62:

Commencing to correct the circuit drawings up to date in preparation for chassis layouts and assembly of the circuitry already proven -

Received a recommended "FIX" from hewlett packard via Radio Wash. for correcting the clock jump when switch to the 1KC position of the meter - will install - test and forward on to Carolina Beach:

Installed the hp "fix" in both clocks

6/1/62: Tested the 1 second clock against timer - could not detect any jump in timing when switched to 1KC meter position or to any other meter position - forwarded info on to LCDR Edwards at Carolina Beach -

Continuing with circuit layouts and chassis design - ordered parts for 100KC amplifier -

W-234 (CONT):

6/1/62 (CONT): Continuing with breadboard and test of the FPN-38 timing circuitry -

6/4/62: Continuing with chassis design - W.O. to lab to build chassis to hold ϕ shifter, 100KC amp and basic timing circuitry

Laying out circuits to be put into trans. - sending to Calbig in lab for possible printed circuit layout.

Correcting all schematics to come up with a smooth copy to work from:

Starting to run in monitor lines from the timer to the monitor panel (divider used, Mg stard and trans. triggers after two trigger selector) through cathode followers as necessary to preclude loading down timer: timer tied up so this may get delayed:

6/5/62: Seared on running monitor lines due to time obligations - Plan to build anticipated Cathode Followers for Mg stard; xmtr triggers and for divider used:

Assembled available clock, scope and power supply for FPN-38 project into its cabinet

Cont. work on FPN-38 logic/timing circuitry -

Finished up master schematic for FPN-41 timing and trigger insertion circuitry - sketch of timing cabinet front panel and switch location drawn up.

Progressing on fabrication of timing drawer to house phase shifter and timing circuitry

Laying out printed circuit configuration for the part of timing project going into transmitter drum drawer.

W-234 (CONT)

6/6/62: Lab continuation fabrication of timing chassis drawer and layout of printed circuits

Picking up ends on ordering of needed parts — continuing to pick up monitor/reset signals from timer so as to cause no mal function or fed back into timer — Ms start taken off OK w/o need of C.F. — X111TR triggers taken off OK w/o need for C.F. Constructed C.F. for DIVIDER RESET / DIVIDER CLEAR triggers

Completed initial breadboard of FPN-38 reset circuitry and letting run for test:

W-234 (CONT)

6/7/62: Cont. oper test of breadboard set up (NOT IN TIMER) of FPN-38 reset circuitry — oper OK @ 0800 — 0930 tested & circuit failed — Cont. adj of monitor outputs from timer — working on the half of ~~divider reset inhibit with~~ the cathode follower involved with divider reset to eliminate capacitive effects of long cable to monitor panel causing definite decay of the slope of the pulse — plan to change the cathode R to about 22K and couple out with a very small capacitor — deferred this due priority use of timer on dicca project

Completed timing chassis returned from lab and fitted into timing cabinet: Work cont. on printed circuit part of timing circuitry

Preparing schematic of all timing circuitry on the timing room board in preparation for re-hooking up the breadboard and cleaning up the circuits —

Continuing on FPN-38 breadboard to clean up and test circuits and get proper inhibit waveform —

6/8/62 Tests with "divider reset" cathode follower shows that it is not practical to achieve desired waveform out using the CF — need low RK & with the negative pulse, we get large currents so decided to use voltage divider off with small coupling capacitor — looks OK — started building this small CF (divider clear) and voltage divider (divider reset) into vector turret card

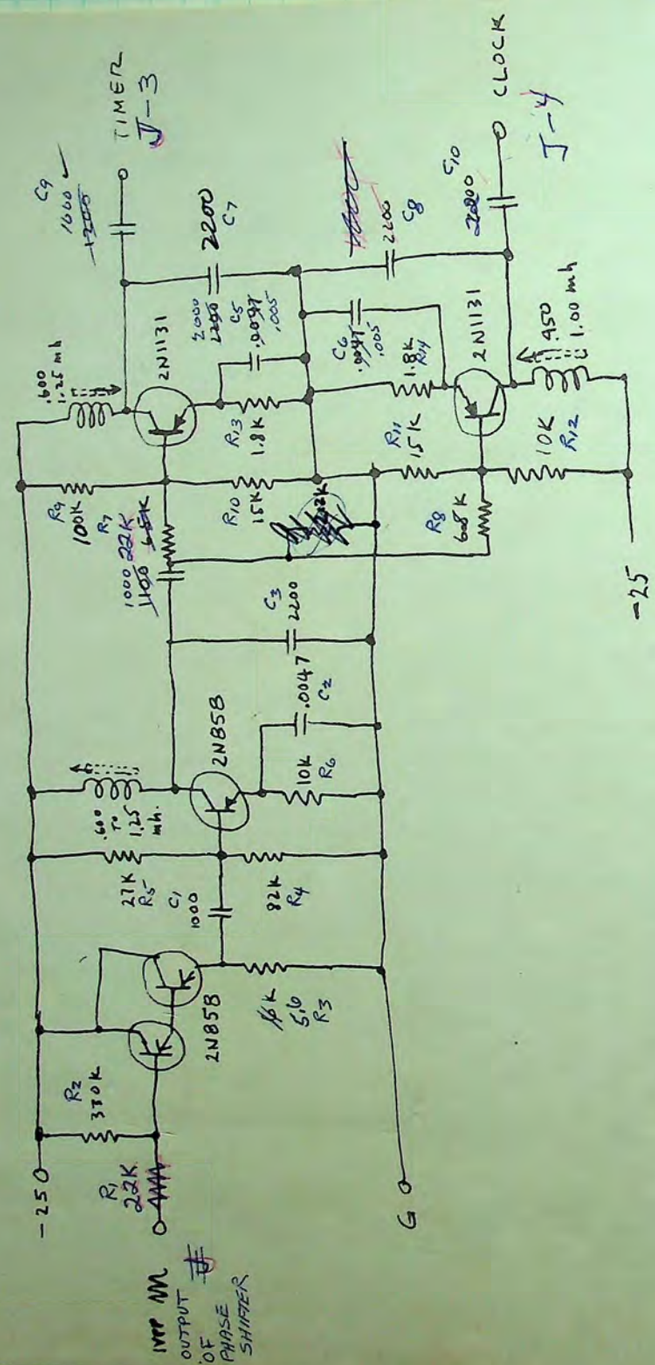
Picking up some more ordering for timing chassis — schematic on timer room board finished — layout 100 KC amplifier for printed circuit — saw spikiness on 100 KC out of amp if compared to 100 KC in and got the same spectral components out — so feel 100 KC amp is linear enough —

6/11/62: Started construction of timing cabinet chassis — rec'd filament transformer and barrier strips — ordered few parts orig. ordered from Vary but not received — Installed divider-clear and divider-reset takeoff circuitry (cathode follower and resistive divider) package into divider drawer — appears OK —

Performed addl tests on 100 KC amp — appears OK on spectrum analyzer — lab starting circuit board const.

W-234 (CONT)

100KC AMPLIFIER (MOD-C) FINAL 6/11/62 JFE



W-234 (CONT)

6/11/62 (CONT): Readjusted the 100KC amplifier - retuned and measured harmonics with spectrum analyzer -

2nd harmonic: 42 db down from fundamental
3rd " 50 db " " " "

Call from BARSEN - FPN-38 part of timing is better than FPN-41 part - want data on expected heat dissipation and power requirements for 38 timing rack - preparing to check same - putting all gear into timing rack - and then into timer room -

Corrected schematic & preparing to test breadboard on FPN-41 circuits to reduce some component values to more realistic figures plus get desirable inputs off the circuits

Work progressing on the printed circuit boards for FPN-41 in timer circuitry - continuing on const of timing cabinet chassis -

6/12/62: All gear set into FPN-38 timing cabinet in preparation for making heat dissipation tests tonight (ie ambient temp change in sealed timer room with one FPN-41 running with two hp-160B scopes & timing rack)

Making changes in the FPN-41 reset/timing circuitry to get balanced flip flops & trigger amplitudes established - work continuing on fabrication of the timing cabinet drawer and printed circuits to be installed in tran. drawer.

hp-160B Oscilloscope: 115V or 230V (±10%) ac 50 to 440 cps - 480 watts (ea)

hp-724 BR Power Supply: 115V or 230V (±10%) ac 5 to 1000 ~
temp limitations 0 → 50°C

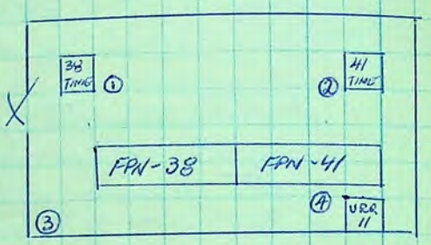
hp-1BBR Clock: 22-30 v dc - approx 2 watts - from hp-724 BR -
temp limitations 0 → 50°C

W-234 (CONT).

6/12/62 (CONT): Continuing to make tests on the FPN-38 reset circuitry - making connections into FPN-38 timer to get desired power & voltages -

6/13/62: RESULTS OF TEST - AMBIENT TEMP. RISE IN TIMER ROOM DUE TO FPN-38 TIMING RACK (ie: 2ea HP-160B SCOPES) - heat dissipation from the two HP-724 power supplies and clocks deemed negligible.

CONDITIONS:
(a) FPN-41 ON XCAL PLATES
(b) URQ-11 ON
(c) 2ea HP-724 & 113BR CLOCKS ON
(d) ALL OTHER OFF
(e) AFTER 6h 35m TURNED ON 2ea HP-160 B SCOPES
(f) ① → ④ indicate locations of thermometers in FPN-38/41 timer room



	TIME	①	②	③	④	REMARKS
	1725	32°C	33°C	30°C	32°C	set conditions ⓐ → ⓓ
① Δt 6h 35m	2030	34°C	34°C	33°C	34°C	stabalized cond. ⓐ → ⓓ
② Δt 7h 00m	2400	34°C	35°C	33°C	35°C	SWITCHED ON ⓔ
	0700	39°C	38°C	35°C	37°C	final reading cond ⓐ → ⓔ turned off scopes
ΔT ②	7h 00m	+5°C	+3°C	+2°C	+2°C	

maximum temp rise: +5°C 35°C = 95°F
min " " +2°C 40°C = 104°F
avg " " +3°C

INFO FOR BAETSEN

or about 6°F temp rise:

two scopes on add 960 watts of power

passed on to BAETSEN via phone on 6/15/62 JOE

Continuing to work on cleaning up the FPN-41 timing chart breadboard - placing the four (4) thermometers into the clocks and power supplies to check ambient operation temperatures.

W-234 (CONT):

6/13/62 (CONT): Continuing to work on FPN-41 breadboard to clean up the negative reset (derived from divider clear) trigger to F.F. #2 - having difficulty with the first negative trigger in the train (and the one which will be used) causing the inhibit waveform out of the F.F. #2 to have an unacceptably long rise time -

Connected FPN-38 reset circuitry into timer and achieved a reset - will have to test now to determine if reset is acceptable -

6/14/62: Tested FPN-38 reset: reset OK (2sec clock) - but with the following difficulties:
① must inhibit M enr servo to positively reset back to same time, as required to divider reset, each time:
② when inhibit as we did (stopping 100KC to "A" divider) the transmitter triggers are also stopped and since thinking of resetting every 4sec, this will be too long a period for transmitter triggers to be missing and thus the kick off XMTR
③ if reset every 4sec, 1/2 PRR should be in proper time to give same phase code on each reset:

The above was using reset system as going into the FPN-41 - ie inhibiting the divider from counting until clock reset time -

Continuing on with assembly of the FPN-41 timing cabinet drawer - also still working with the FPN-41 inhibit F.F. output in the attempt to improve the output waveshape -

6/15/62: Idea put forth for FPN-38 reset: instead of inhibiting the divider and then waiting 4sec for the reset, if can generate a 1/2 pr waveform from the clock, then we can gate thru a desired trigger derived from this 1/2 pr waveform to cause the desired reset in lieu of waiting for four seconds and the true clock pulse - would need a (÷10÷2÷2÷2) logic circuit operating on the 1KC from the clock to get the desired 1/2 prr for rate SLO (12½ PPS ; T = 80,000 usec) -

Contacted transistor module company in Clifton NJ for prices and data on 4X and decade counters - rec'd quote for 4X flip-flop late in PM @ 90.00 ea - plus data being sent to show how the 4X is made into a decade counter -

Prepared req. for procurement for 4ea 4X flip-flop boards plus plan to ask for loan of two ea of these boards to play with (as per phone conversation) -

W-234 (CONT):

6/15/62:

Also went up to the FPN-38 timer with a pulse feeding the divider reset generator in hopes of being able to get a reset simply by application of this clock derived pulse — initial tests showed reset to be near but probably more random than not — more tests needed and data to be collected to confirm where reset is happening.

Work cont. on FPN-41 timer cabinet chassis fabrication and testing on the inhibit F.F. waveform

6/18/62: Called DIGITAL COMPANY, Clifton, N.J. advising them that order being placed for 4ea 4X flip flop boards and requesting loan of two each —

FPN-38 RESET TESTS

Shaped a positive pulse (clock tick) from the two second clock to look exactly like the normal positive input to the AN/FPN-38 reset generator. Applied this to the reset generator and achieved a reset identical to that normally produced by the reset generator — Then attempted to reset the timer divider chain using this clock derived reset —

RESULTS: Unable to get a repetitive reset which would go back to the same time relation to clock info, each time: Reset times were observed which would bear, with respect to the clock derived pulse, time differences between zero and ± several hundred u sec — It was impossible to ascertain ahead of time just where the reset would come & therefore it was RANDOM

Thus the timer divider chain must be permitted to count out the rest of the interval and be reset at some time later with respect to time derived from the clock

The approach now will be as follows:

① from the clock 1KC (triggers or squared 1KC) plan to develope a 1/2 PRR waveform commensurate with rate SLO (12½ prr)

② Then from this 1/2 PRR, develop triggers ~~[illegible]~~ from the leading or trailing edges of the 1/2 prr.

W-234 (CONT)

6/18/62 (CONT)

③ Then using the same principle developed for the FPN-41 (and as already built & given pulmonary test on the FPN-38) a normal divider reset will be gated thru, on the push of a button, to stop the "A" divider.

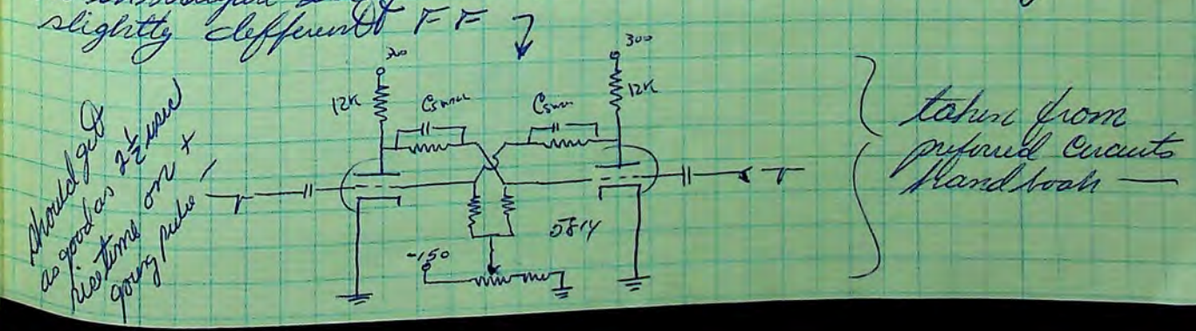
④ Then instead of waiting for a full two (or four) seconds for clock information to start the divider counting, one of the triggers developed from the 1/2 PRR ② will come through to un-inhibit the divider and start it counting again

⑤ Thus the divider will be inhibited for only a short time (say maximum of 4 intervals or 320,000 usec) and will not lose a transmitter due to a long absence of transmitter triggers.

⑥ In addition, the 1/2 P.R.R. flip-flop will also have to be reset at the time the divider becomes un-inhibited (by use of a delayed trigger generated from the trailing edge of the divider inhibit waveform) to insure that we have reset the phase code back to its proper and original condition — since the clock is ~~[illegible]~~ developing a 1/2 P.R.R which should stay in step with a timer, this resetting of the 1/2 PRR should be no major problem

⑦ Also the use of the above scheme will permit the development of a relatively simple "coincidence detector/alarm" circuit which will constantly check both timers against the clock for "in step" tracking to w/in 10 usec —

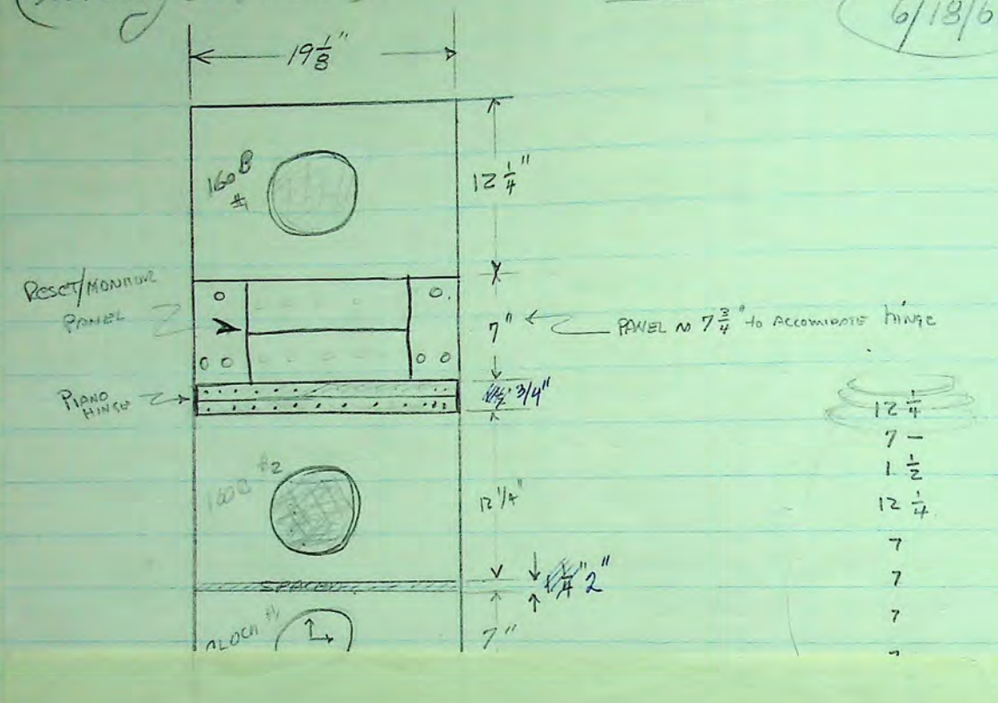
Continuing on with assembly of the FPN-41 timing cabinet chassis and also testing of the FPN-41 timing breadboard to get a better inhibit waveform to feed the 100KC BS driver — plan to investigate use of 5687 tube — also constructing a slightly different FF



(AN/FPN-38 timing cabinet)

equip. mounting space available 70"

6/18/62



(MODIFICATION TO FPN-38 TIMING CABINET EQUIP)

W-234 (cont)

6/19/62: Have ordered parts for 100KC amp (procurement req made upon) but distrib did not issue to "State Electronics Parts" until 6/14/62 with 14da delivery — plan to call for possible speed up — also ordering parts today for the FPN-38 timing/reset circuitry (as tested already) —

W.O. to lab for the second FPN-41 timing chassis — still working on new inhibit F.F. circuit:

Data taken on the 0202 - 100KC oscillator output impedance and the load presented to this oscillator by the (two) FPN-38 timer connections alone and one and two Hp-113BR Clock/freq divider — used method of equivalent resistance to reduce oscillator output to 1/2 its open circuit value —

results from mason two diff. 0202's

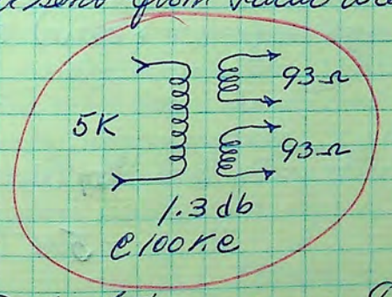
APPROX Z_{OUT} 0202 OSC = 4K E_{OC}=120 E_L=60V

APPROX Z_{LOAD} ADDED BY FPN-38 = 2.7K E_{OC}=120 E_L=50V

" " " " (1) CLOCK = 200 Ω E_{OC}=120 E_L=8V

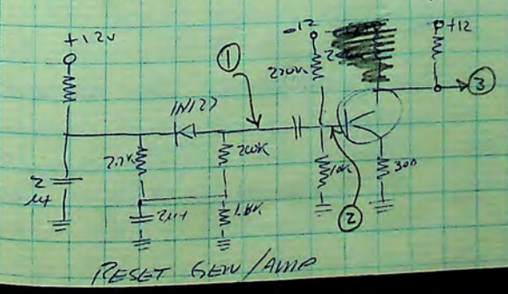
" " " " (2) " = 120 Ω E_{OC}=120 E_L=4 3/4 V

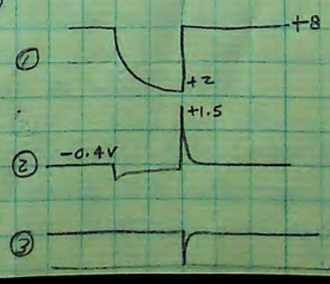
Asked for the impedance matching transformers (as shown) to send from Radio Washington:



(advised on 6/19/62 that they are on the way:)

Data taken on reset pulses of FPN-38



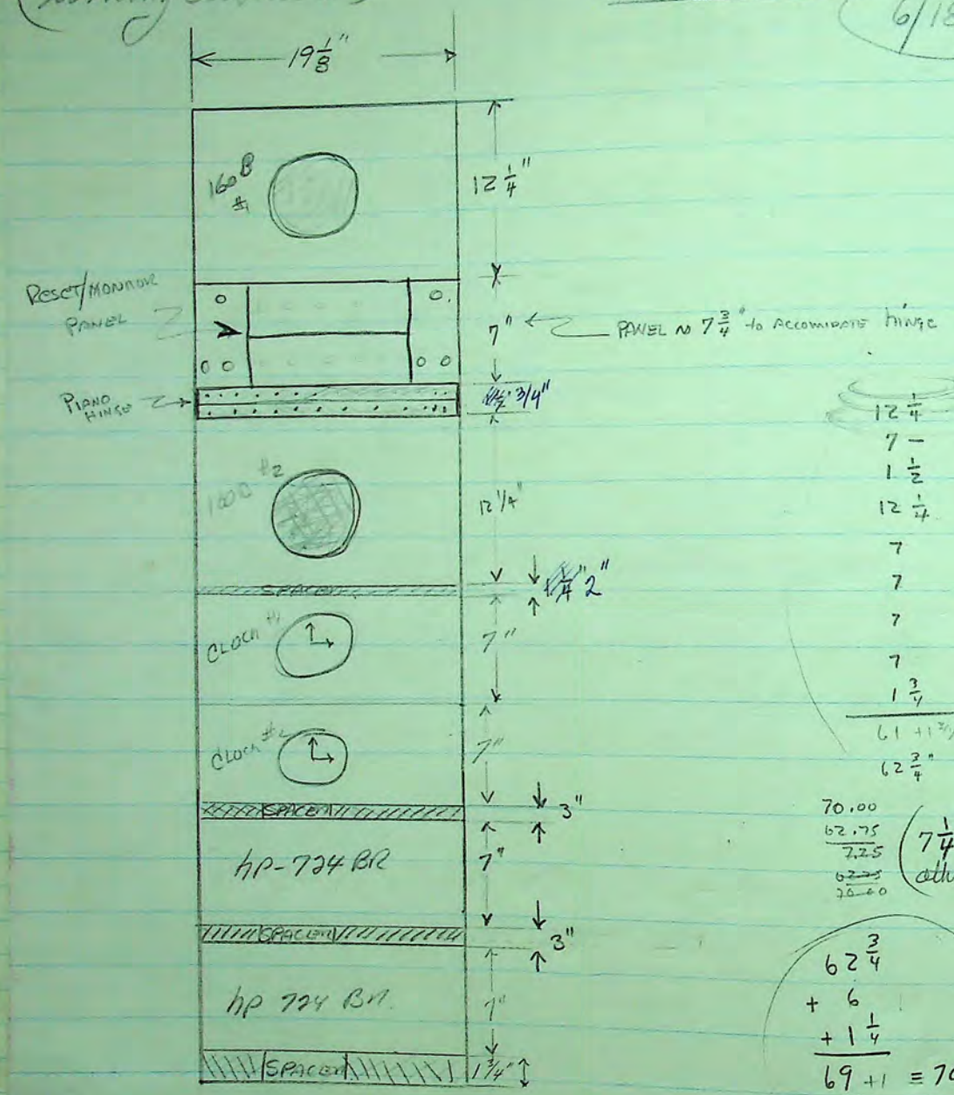


(RESET OUT)

(AN/FPN-38 timing cabinet)

equip. mounting space available. 70"

6/18/62

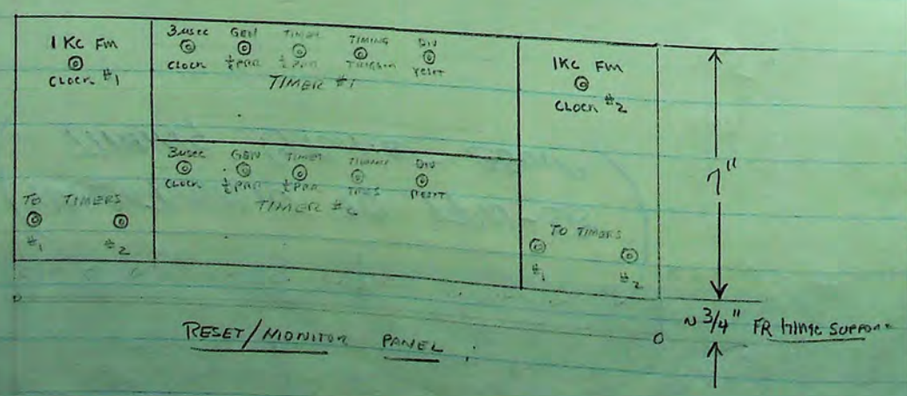


12 1/4
7
1 1/2
12 1/4
7
7
7
7
1 3/4
61 + 1 3/4
62 3/4"

70.00
62.75
7.25
~~62.75~~
~~70.00~~

(7 1/4" for all other spaces)

62 3/4
+ 6
+ 1 1/4
69 + 1 = 70"



RESET/MONITOR PANEL

W-234 (CONT)

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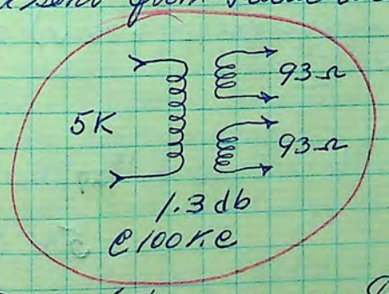

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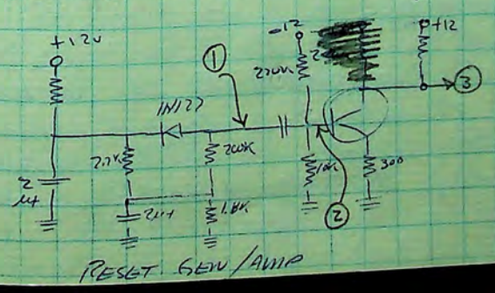
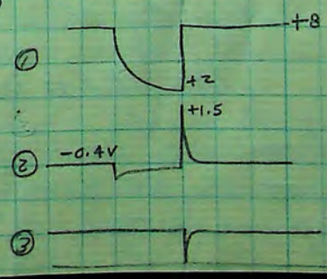




(RESET OUT)

W-234 (CONT)

6/19/62 (CONT)

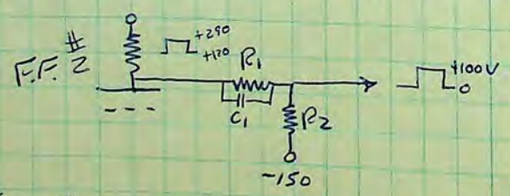
Testing slightly different inhibit FF (#2): this has grounded cathode with grids returned to -150 (divided) — same 5814A tube — tests show problems with the impedance presented on the trigger input circuit causing the signal coupled over from the opposite plate to be lost (ie into too low an impedance due 2 presented by trigger circuit) —

6/20/62: Coupled trigger into FF #2 thru diode — this appears to correct F.F. problems and it works OK & w/o commutating capacitors (180V signal) — application of 20-40 pf of commutating capacitance gives a nice 1 to 2 usec rise of pulse — amplitude ~130V — should have more to compensate for voltage division down to -150V (to get a 0 → +100V inhibit pulse) — varying value of the plate to grid and grid to -150 resistors to get a better RC between commutating elements:

Continuing work on 41 timing chassis — fabrication of the second chassis has commenced: —

Majority of components for the 100KC amp & the FPN-38 read circuitry have been ordered — the two F.F. boards have not yet been rec'd nor have other parts — drawing up requirements for small power supply for FPN-38 - clock/½ PPR divider circuitry —

Coupled the INHIBIT FF #2 waveform (~ 120 → 290 V) thru a 1M variable resistor to -150V



∴ R1 ≅ 2.2M
R2 ≅ 2.8M
for (0 → +100V PULSE)

$R_1 \cong 12/27\,(R_1+R_2)$

$R_1+R_2 = 5M$ (POT):

$C_1 \cong 200$ pf.

Achieved a good (~ 2 usec) rise and fall of the inhibit waveform:

Attempted to couple this waveform into the 100KC section of the divider — unable to achieve a desired inhibit of the 100KC-BST by direct, diode or resistive coupling into the BST switching grids, BST driver cathode or 100KC squarer cathode:

W-234 (CONT):

6/21/62: Will attempt now a slight variation for causing the FPN-41 divider to stop on reset and start on the negative timing pulse: using the POSITIVE going inhibit waveform, will differentiate to get a POSITIVE going trigger (FIRST ONE) and a NEG. going trigger (SECOND ONE) — Then apply the (+) to the cathode of the 100KC-BST to extinguish the beam and the (-) to Spade #9 to reform the beam at the time of desired reset.

Measured the time difference existing between normal divider reset and the time of start of the inhibit pulse (F.F. being triggered by a gated & inverted divider clock trigger) — there appears to be about ½ usec delay before the start of the inhibit pulse up and due to slope of the leading edge of the inhibit waveform, about 2 usec additional before the pulse will reach full amplitude — This should be time enough for the (+) inhibit pulse to hit the BST cathode after normal divider reset has formed the beam on spade 9, and extinguish the beam again (ie do not want the inhibit pulse to extinguish the beam and have normal divider reset thru at the same time to reform the beam) — This will include having to stop the 100KC amp; squarer and BST driver (BST will not switch if beam not formed) and there should be no delay in getting the divider going again at the time of desired reset (un-inhibit).

FPN-38: necessary to have (-)15V to run the 4X & 10X modules — boards themselves will draw about 200 ma — if voltage divide the (-) 28 V available in the timer to (-)15 this will cause additional (est as much as 300 ma) drain on the ±28V power supply — under normal operation, timer draws about 440 ma from the (-)28V half of the timer-power supply and power supply is rated at 1.5 amps:

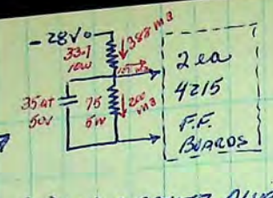
∴ 440 ma + 200 ma + 300 ma = 940 ma

The power supply should be able to take this load — plan to check out today — if not then addl power supply must be provided (built) —

Calling Mr David Pinniston @ DIGITAL EQUIP CORP. today to see if he can expedite delivery of both the borrowed modules and the 4 modules ordered from his company. — received digital logic handbook from him on 6/20/62 —

W-234 (CONT)

6/21/62 (CONT):



Loaded down the FPN-38 (-) 28V power supply with an equivalent resistive load equal to or greater than it is expected the timing circuitry will load - about 0.9 amp taken off (including normal timer requirements) and it is felt this is not too excessive (P.S. rated @ 1½ amps) - plan to go ahead and not build addl. power supply

Still attempting to couple in the FPN-41 inhibit waveform or trigger to 100KC-BST circuitry - attempted to couple in the following ways - in each case, the problem resolves down to one of achieving an adequate impedance match in order to couple in the desired energy to do the job:

(a) Pos. INHIBIT ⊐⊏ ON TO 100KC-BST SWITCH GRIDS @ C9 & C10

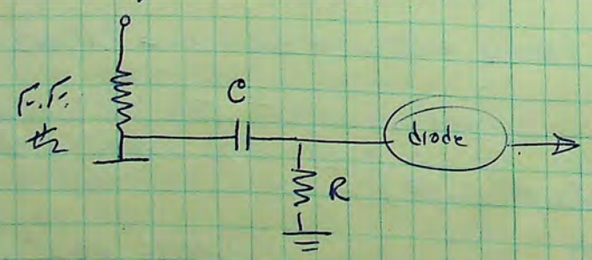
here Z looking back toward inhibit circuitry appears to be too small compared to the hi Z grids & the switching waveform amplitude degenerates immed. on hook up - also inhibit waveform not effectual (will go back to this)

C = .35μf
R = 2.2 → 5M

(b) Pos INHIBIT ⊐⊏ on to cathode of V2B (100KC square) - here load of cathode < inhibit load & inhibit waveform degenerates to point of no effect

(c) Pos TRIGGER ⊥ on to cathode of 100KC BST - again Z looking into is too small & trigger ampl reduces below value necessary to cause desired action: (ie clear the tube)

plan to change (increase) value of the capacitance coupling off the INHIB. F.F. so can decrease value of Bleeder to get better impedance match



W-234 (CONT)

6/22/62: Started to work on the inhibit of FPN-41 but timer had to be used for decca project & secured early in AM -

Another plan to cause FPN-41 inhibit is to feed the 100KC BST cathode with a large (100+V) trigger to turn off the beam immediately after the normal divider clear/reset has caused the beam to form on spade 9 (& shift to 0) - then at the time of the standard (or delayed standard) second, hit spade 9 with a negative trigger to cause the beam to form again - this precludes having to stop or interfere with the 100 KC driving signals to the BST and should give a ~~[illegible]~~ reset which occurs at the time of the standard (or delayed standard) second - going ahead and building a THYRATRON pulsegenerator, keyed from the timer, to give a good positive trigger to work into the relatively low impedance BST cathode

The wiring has been completed on the first FPN-41 timing chassis and is being set up for test & shakedown - tested out chassis - all OK except for shape of the "one sec" negative timing pulse out (distorted - too long) - this is a coupling and impedance problem so plan to connect up the long length of RG-59B/U cable thru which this pulse will have to run to timer (from reset panel) and then work this problem out:

Timer still tied up all day with W-232 - FPN-38 Parts not ingot

6/24/62: TAC conference - briefed CO up to date on project for his trip to HQ.

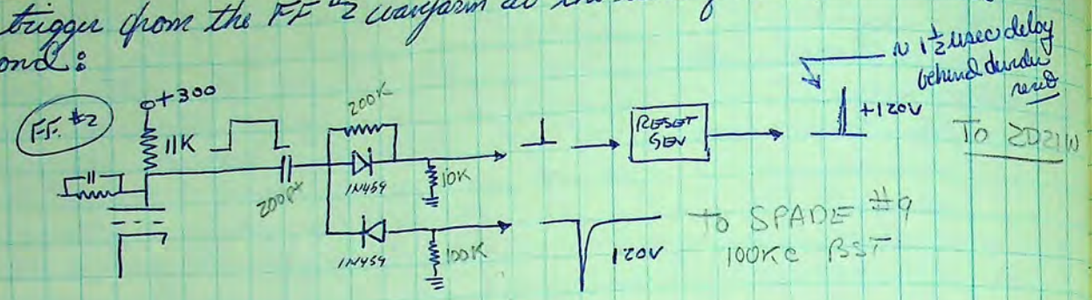
6/25/62: Timer allocated to W-232 (decca blanking project)

Connected up the 2021W reset generator driven by a positive trigger derived from the (+) going inhibit signal from F.F. #2: - trouble coupling off this pulse and still maintaining a sufficient negative trigger (100V+) to be used on spade No. 9 (as discussed above) - also the timer reset generator has a natural period of around 5cps (T = 200,000 usec) so had to connect a large resistor from B+ to the cathode to stop this - finally achieved the desired coupling, differentiating & impedance matching of information from F.F. #2 to cause the reset gen to work properly and to give a good neg

W-234 (CONT)

6/25/62 (CONT):

trigger from the FF #2 waveform at the time of the standard second:



This should give us a good (+) trigger into the relatively low impedance cathode (~4K) of the 100KC BST and a good negative trigger onto the high impedance spade #9 of the 100KC BST. - will test when can get timer:

Continuing on with connecting up info from the timing cabinet so can get fixed values set to give desired info out - running the RG-59B/U cables that the one sec timing pulse will look into and connecting patch board for clock info to timing chassis.

Second timing chassis const & incl. of parts started

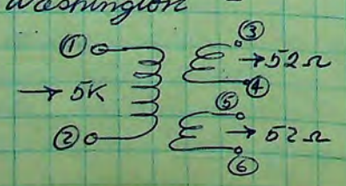
6/26/62:

Completed initial testing of the first timing chassis (FPN-41) - obtained acceptable "NEG TIMING" pulse to operate flip-flops; acceptable "LSTS A00" waveform thru long length of cable (as will be going to timer) - will have to shape the "ONE SEC" trigger going to the timer after run thru long length of cable -

Can now disassemble the vector board set-ups xcept for the circuits to be on the printed boards -

Setting up to test LSTS add circuit when can get use of the timer (still obligated to W-232):

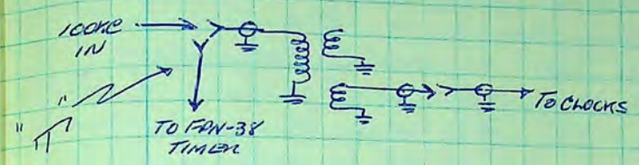
Received two (2) ea, 100KC matching transformers from Radio Washington -



W-234 (CONT)

6/26/62 (CONT):

Breadboarded 100KC transformer as shown below & connected to 0202 osc in FPN-38 & to the cable leading to both clocks



① w/ timer conn to osc alone, $E_{osc} \cong 48V$ p-p

② w/ osc output to XFMR & "T" to timer $E_{osc} \cong 50V$ p-p

③ E_{out} to clocks $\cong 3\frac{1}{2}V$ p-p (sufficient to drive both clocks)

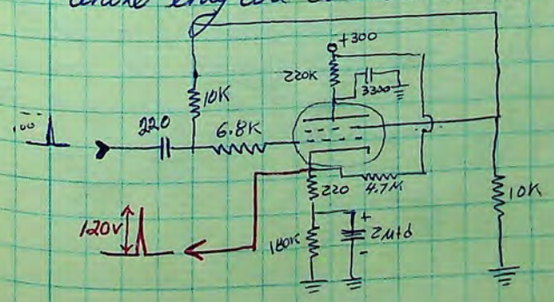
∴ This appears not perfect but acceptable means to take 100KC to timer & low input clock from one osc & thus will have small cans built to contain input/output plus XFMR suitable for mounting on cabinet near 100KC osc

Digital modules did not arrive today - timer occupied all day (FPN 41) with decca blank project -

Fabricated reset gen from breadboard of timer divider clear pulse generator - connected up & satisfactorily tested:

Found FPN-41 divider reset gen has natural period of approx 0.7 sec - by adding 30 mfd to the 5 mfd capacitor in cathode could extend period out to 1½ sec or sufficiently to allow one(1) sec reset if this methode used -

6/27/62: Using set up on opposite page and the fabricated reset gen, attempted various means of resetting the divider (FPN-41) by pulsing cathode (+) and spade #9 (2) immed. after divider reset (normal) - finally achieved the amplitudes needed in the (+) & (-) pulses where they are connected in the circuit:



2D21W RESET GENERATOR:

gives good low impedance output positive trigger for use as a clear pulse on the cathodes of BST's

W-234 (CONT)

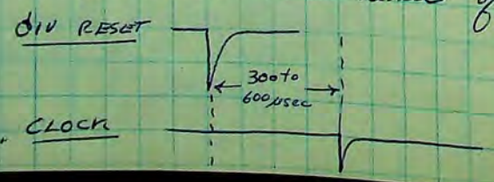
6/27/62 (CONT): Attempts to reset 100KC BST with "reset" and "clear" generated from the inhibit FF #2 output

① applied clear (+) pulse to cathode of 100KC BST thru C-12 removed from ground — C12 too small so substituted 0.22 mfd cap — could satisfactorily clear BST providing the normal timer divider reset was disconnected from the tube @ junction of C13, R47 and R48 — with normal divider reset occurring about 2 usec ahead of the applied clear pulse and being about 15 usec wide, the applied clear is ineffectual in extinguishing the beam (ie amplitude of the reset pulse on spade #9 is still quite large after 2 usec & the beam is held on spade #9)

This could be corrected by delaying the applied clear pulse by 5 + 10 usec or by lengthening out the applied clear pulse duration or by sharpening up the divider reset pulse to make it much narrower (say about 2 + 5 usec wide) But there are other problems

② Applied a reset (−) pulse to spade #9 of the 100KC BST at junction of R-47 and R-48 ; through a 2200 pfd capacitor - the BST could be reset with this pulse but it was in the cleared state however with the normal divider reset line connected, the tube could not be properly cleared to make operational test but with divider reset line disconnected the BST could be cleared & reset with the trigger derived from the inhibit waveform:

③ By disconnecting the normal divider reset line as noted above, in ①, and letting the divider get started properly on rate S Ø, could get divider reset in synch with the clock pulse (at some random relation) — then upon hitting the reset button just before the one second clock trigger was due, could reset the divider to within 300 to 600 usec of the clock but no closer:



W-234 (CONT)

6/27/62 (CONT):

The problem, apparently, is this: the inserted clear coming just after normal divider reset (~2 usec later) properly clears the 100KC BST (which now has normal divider reset disconnected from it). Normal divider reset has also reset the 10KC BST and the beam jumped to T Ø immediately on reset. Thus when our inserted clear comes along to the 100 KC BST, the Beam in all probability is on spade 9 or just going to spade Ø, and when the beam is extinguished, this may send a trigger to the 10KC BST driver causing the 10KC BST beam to jump to target 1 — with the 100KC BST now OFF (Beam extinguished), the divider is STOPPED but instead of the beam in the 10KC BST being on spade (target) Ø as desired, it is probably on target 1 — then at the time of the one second reset pulse derived from the clock, a negative reset is inserted onto spade 9 of the 100KC BST and the beam jumps on 9 and shifts to spade Ø immediately — this puts another trigger to the 10KC BST driver and the beam jumps to target #2 of this BST — This is supposed to be time 0 now and 100KC trigger cause the 100KC BST to commence counting and when it comes around in its normal counting sequence to the transition (switch) from spade 9 to spade Ø, a trigger goes again to the 10KC BST driver and the 10KC BST beam jumps from target #2 to target #3 instead of from target Ø to target 1 as we desire — thus we pick up at least 200 usec time difference here between the time of the standard second and the time of divider reset. The additional time (300 to 600 usec) is probably due to some other transient triggers getting to the 10KC BST driver causing the beam in that BST to be somewhere between target 3 and target 6 at the time the 100KC BST starts its normal count again

CONCLUSION: It appears that this method of achieving divider reset would be undesirable as it would involve going into the divider and into each BST with a different clear/reset approach than is normally used —

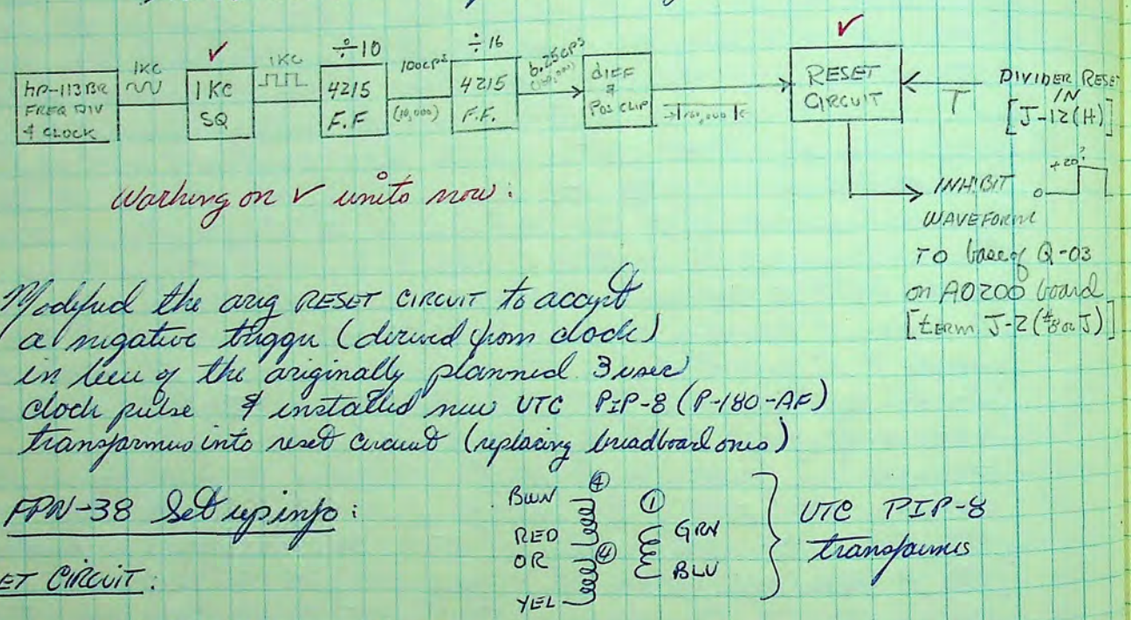
Now plan to return to the original idea of inhibiting the 100KC going to the 100 KC BST driver or inhibiting the driver itself: The problems of previous tests of this nature may be resolved by extending the natural period of the timer divider reset out to 1½ seconds (see page 101)

W-234 (CONT)

6/27/62: Called DIGITAL EQUIP CORP on the modules they are sending on loan – they stated the boards were mailed parcel post (special handling) on 6/25/62 and should be here today or tomorrow.

Planning to get all circuits possible breadboarded except the F.F. modules in hopes we can save some time.

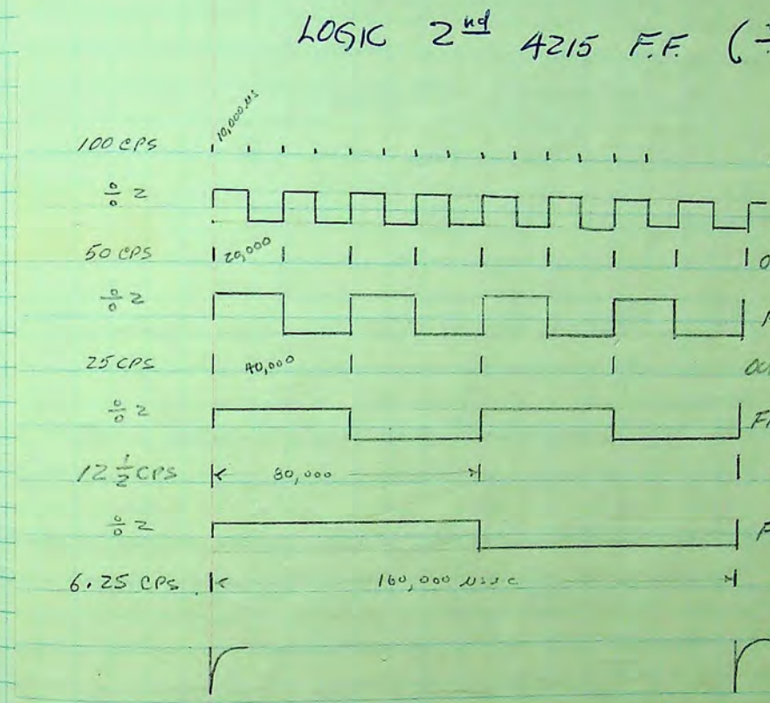
The overall FPN-38 plan is as follows: (RATE SLØ)



W-234 (CONT)

6/28/62: Disassembling FPN-41 used breadboard xcpt for the FF's & used circuits not already assembled in prep for further tests of interfacing the 100KC end of the divider – restored FPN-41 timer to normal condition after 6/27 tests on 100KC – BST.

Plan to continue on with setting up FPN-38 circuitry to accept 4215 boards



Continued to work on the FPN-38 used circuitry – changed input circuitry to accept a NEGATIVE trigger as it is planned to have available from the ½ P.R.R. waveform (see above) – to have available from the ½ P.R.R. waveform (see above) –

Some difficulty with this circuit – SKUTINS on leave today

W-234 (CONT):

6/29/62: Cont. to work on the FPN-38 reset breadboard — having some difficulty getting F.F. to work as before —

Received 4BIT modules (on loan - 4 ea) from the Digital Equipment Corporation today — started to set up these with needed voltages to test

7/2/62: Cont. to set up 4Bit Modules for test — unable to achieve the needed fast rise time (~0.2 usec) in the input 1KC trigger (of square wave) derived from the clock — tested the 4Bit board (wired for decade division) with a 1KC square wave input from a square wave generator having a fast (+) going waveform and achieved very satisfactory operation - will have to design a new 1KC squarer (were using copy from FPN-38 timer) which can give us the desired fast rise waveform to drive the divider.

The cleaned up FPN-41 inhibit/gating flip-flops on the breadboard were tested & appear to operate O.K. — as have time, plan to cop. (large) into 100KC section of the FPN-41 divider (100KC end) to get desired inhibit of the divider

7/3/62: Picked up the lab sq wave gen & fed into 4215 board (decade divider) @ 1KC — board operated OK — then connected up the ÷16 board and it operated OK —

Still working on generating a good enough (< 0.2 usec) rise time 1KC square wave to run the 4215 boards —

Difficulty finding dc power supplies — now going to set up the boards adjacent to the FPN-38 timer so can pick off needed voltages —

Plan to breadboard a 1KC sq wave gen (from model of 100KC square wave (squarer) from FPN-38) and feed this into the 1KC clipper and amplifier board (# 13A2A 0400) from the FPN-38 — then attempt to pull off the needed 1KC signal to fire the 4215 board.

W-234 (CONT)

7/5/62: Setting up equip behind FPN-38 timer - piping needed dc voltages to set up - getting set up to wire in 1KC squarer and 0400 board —

Called Eric Roth @ WRS on the hp-equip being sent - he advised it has already been sent — will check —

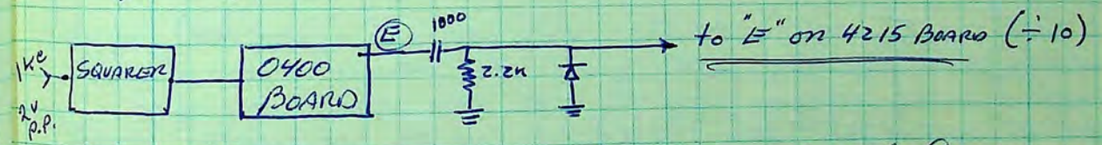
Measured ambient oper. temps inside hp-113BR clock and hp-724BR power supply:

H06 & H07 (113-BR) clocks = 26°C

hp-724 BR power supply = 28°C

Rec'd hp-724BR power supply and hp-160 scope from WRS — clock still to come:

Connected up the FPN-38 - 0400 board fed by output of the copied 100KC squarer from FPN-38 - then fed 4215 board (wired as decade divider) with output "E" from 0400 board thru following network:



holding voltage lowered to ~ 8 VOLTS & could get decade and ÷16 boards to operate OK producing 1/2 P.P.R waveform — also operating 4215 Board @ -12V in lieu of -15 — operates OK:

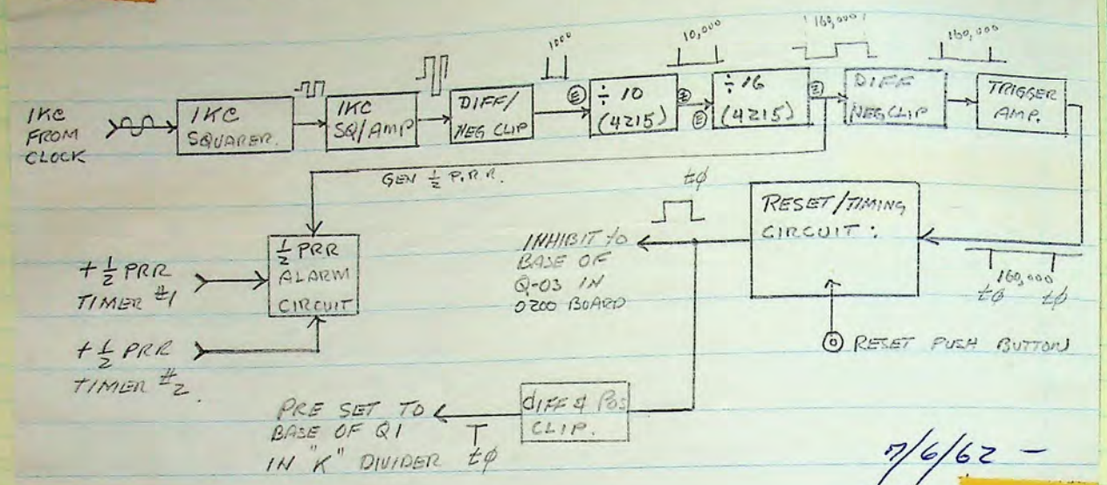
But if bring holding volts up to +10V — no go:

Need an amplifier after the 1KC squarer in order to drive 4215 board — plan on trying the amplifier associated in the 0400 board to do this.

Working on getting the FPN-38 timing cabinet equipment into place for spacing & to establish criteria for having mounting/wired panel made up:

U-234 (CONT):

FPN-38 BLOCK DIAGRAM: 7/6/62 JRC

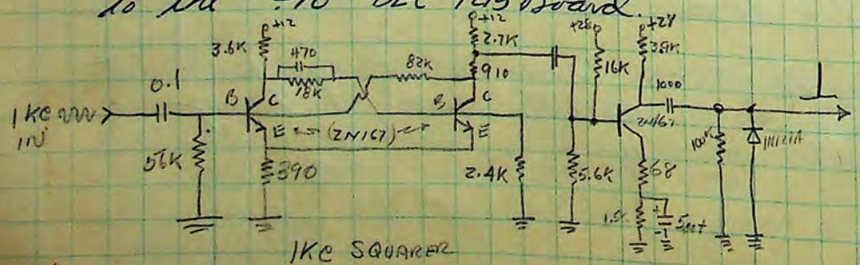


7/6/62 –

7/6/62: The HP-113BR Clock and specific products receiver arrived from WRS in AM – Continuing on with fitting equipment into the FPN-38 timing cabinet.

Continuing to work with the ½ P.R.R generator (from 1KC) circuits – building an amplifier taken from the FPN-38 0400 board to get desired triggers for the ÷10 4215 board – also plan to investigate the 1KC squarer in the 1K selector board (BA2A 0800) for operating on the 1KC out of the squarer already built – will need a trigger amplifier out of the ÷16 4215 board so plan to try the trigger amp. as in the FPN-38 (0800 board).

The use of the 1KC squarer (taken from the 100KC squarer on the 0200 Board) and the amplifier taken from the 0400 board appears to give desirable and satisfactory triggers to the ÷10 DEC 4215 Board.

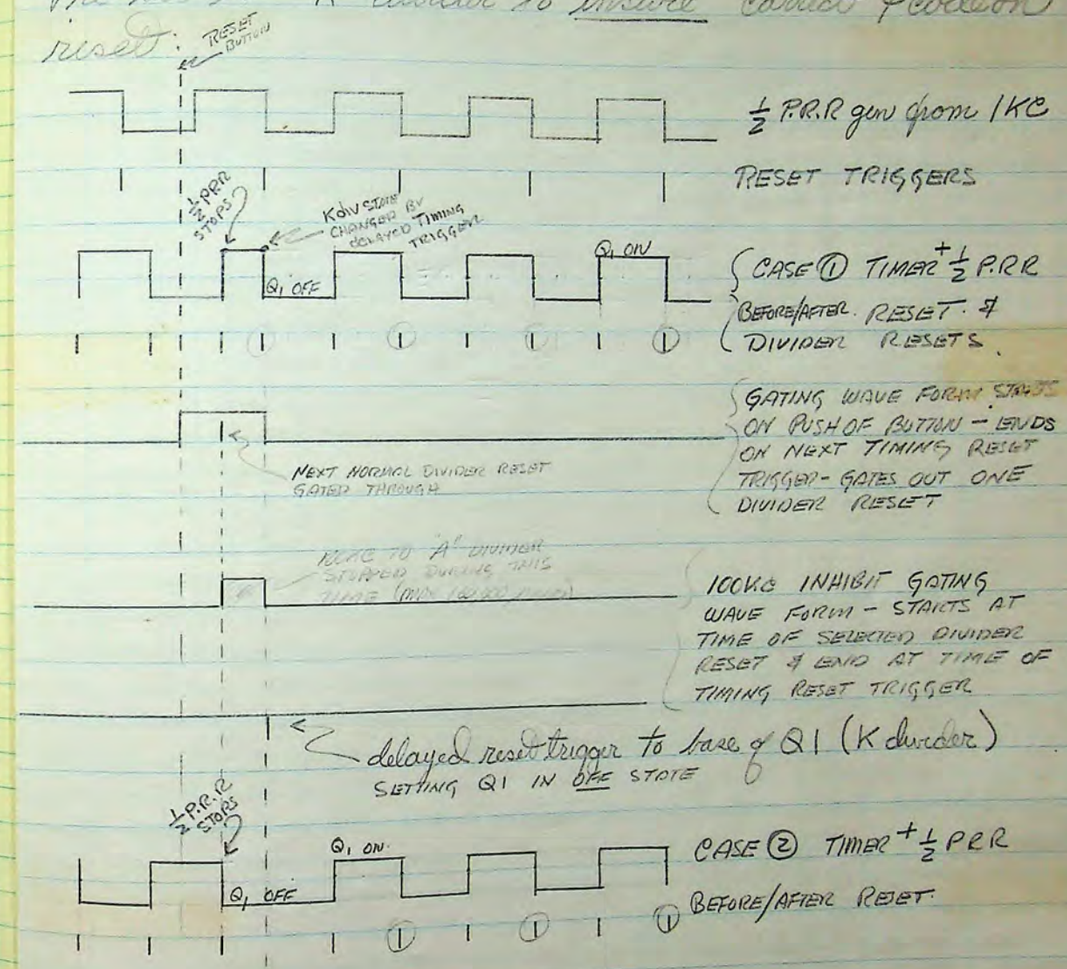


OK

U-234 (CONT).

7/6/62 JRC

Pre-set to "K" divider to insure correct φ codes on reset:



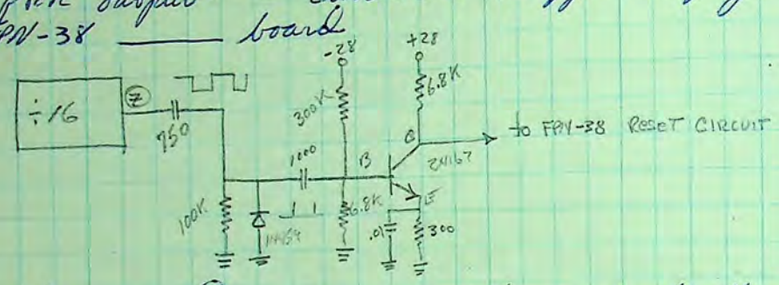
∴ AFTER MANUAL RESET, THE TIMER ½ P.R.R WILL BE IN STEP WITH THE ½ PRR GENERATED FROM THE CLOCK 1KC:

W-234 (CONT)

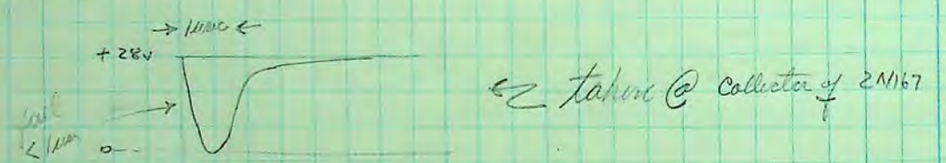
7/6/62 (CONT):

fed output (Z) of ÷10 board to (E) input of ÷16 board and a corrected 1/2 P.R.R waveform produced at the output (Z) of the ÷16 board. (rate SLO - 80,000 usec)

Constructed differentiator and negative clipper for operating on 1/2 PRR output - constructed trigger amplifier from the FPN-38 ——— board



above circuit produces negative resets to the reset circuit as follows:



7/9/62: Set up the transistorized FPN-38 reset/inhibit circuitry on breadboard and fed in the above timing pulse as well as the timer divider reset, - having trouble getting the two flip-flops (2N1214's) to operate properly - made up complete as is schematic - continuing

Fitting together the FPN-38 timing cabinet equip to get all gear in of properly spaced - preparation for ordering the finished reset/monitor panels -

Checking on parts already ordered -

7/10/62: Continuing to check out the reset/inhibit circuitry - still having trouble. Cond. on setting up reset/timing cabinet.

Basic chassis to hold DEC-4215 Boards have been made up and proceeding to wire them up - terminal strips mounted on back/side of the 4215 holders will containing circuitry for feeding the 4215's as well as the reset/inhibit circuitry -

W-234 (CONT)

7/10/62 (CONT): The 100KC amplifiers (FPN-41 phase) have been wired up, but for transistors holding up on this completion till get FPN-38 phase rolling along

7/11/62: Completed setting up FPN-38 timing cabinet equipment location and fitting of monitor/reset & blank panels - made up drawings for forwarding to WRS for finished panel construction - plan to give to LCDR Gobel for hand carry to LT Bartsen -

Phonecall to LT BARTSEN: requesting extension on FPN-38 phase - he advised project extended to 1 Sept 1962 - letter to follow:

Cont. to de-bug the FPN-38 timing/reset breadboard - still having trouble getting an acceptable negative trigger upon pushing reset button -

Going ahead with design and fabrication of an alternate FPN-38 reset/breadboard using standard two transistor (2N167) flip-flops and along the same logic as before - this is in anticipation that the one transistor (2N1214) circuits do not meet operational and stability requirements of the project.

Added distilled water to HP-724BR power supply batteries - found all cells low: - charging them

Modified the two HP-113BR (H07) - two (2) second clocks by bringing 1KC (CW) from front of panel to AUX pulse jack on external back:

7/12/62. Found that the two (2) second pulse from clock is feeding in on the modified 1KC connections made yesterday, causing the 4215 divider to jump 1000 usec every two seconds - must find another way to get the 1KC to the 1KC selection panel.

Succeeded in getting the FPN-38 timing/reset circuit working as desired - put inhibit into timer and achieved acceptable, repetitive reset back to the timing of the clock - testing overnight to see if will fail -

Completed assembly of the divider and trigger circuitry,

W-234 (CONT):

to feed the FPN-38 reset circuit, on chassis suitable for mounting into the timer synchronizer. - Cont. to clean up.

Took mod. out of hp-113BR clock & restored any pulse output as originally run - running 1KC from front of clock back thru a blank panel (BNC fittings) to the 1KC selection board

7/13/62: Continuing to clean up the FPN-38 timing cabinet installation - drilled several hole in top for ventilation - cont. with maintenance cleaning, filling & changing of the hp-724BR power supplies -

Reset circuitry (FPN-38) still working O.K. - Cleaning up and standardizing components where can - modified one of the "K" divider boards to accept a pre-set pulse in order to insure that the 1/2 PRR waveform is in the same state upon each reset - will test later - ran several coax cables out of timer to get info to breadboarded reset circuitry -

7/16/62: LT Bateson here from H.Q. - showed him the progress to date - starting to scan bit parts req. already and on hand in preparation for building first engineering model of FPN-38 reset circuit - Cleaning up FPN-38 reset circuitry in attempt to arrive @ some standard component sizes -

Had some trouble with the 2N1214 transistor F.F. - would not trigger properly - went thru all used ones w/o success - put in new ones & all OK - setting up for putting heat on the circuit -

Finishing up design FPN-41, 100KC amplifiers - Connecting transistors -

Continuing to parallel design & breadboard of FPN-38 timing/reset circuit using 2N167 (common in FPN-38) transistors will decide on most stable circuit later:

Plan to have a heat lamp put on the FPN-38 breadboard from midnight to 0800 for failure tests:

W-234 (CONT)

7/17/62: Circuit (FPN-38) operated OK with temps @ about 98°F @ 0800 this AM - applied more heat (up to about 120°F) and circuit stopped - added commutating capacitors across trigger coupling resistors & they worked OK - finally used various methods of diode coupling in trigger to the two flip flops:

Cont. with FPN-38 timing cabinet equip installation - rounding up parts needed for assembly of the FPN-38 timing/reset circuitry - laying out the remaining circuits for the FPN-38 reset chassis -

Run temp tests on FPN-38 reset circuit (breadboard):

Time	Temp	REMARKS
Ø	36°C (97°F)	operation OK
Ø+10 min	43°C (110°F)	STOPPED - INHIBIT FF gave running due gate FF cont. open
Ø+15 min	35°C (95°F)	operation OK
Ø+20 min	38°C (100°F)	inhibit F.F. becoming erratic - gate FF operation OK
Ø+22 min	41°C (106°F)	gate F.F. operation OK but inhibit FF. goes up & will not come down (remains in the "INHIBIT" state) - immed on turning off the infared heat lamp, the F.F. falls to its normal state & operation although not perfect is acceptable

Conclusions: Below this circuit using the 2N1214 will perform satisfactorily up to temperatures of 100°F - at these temps, the FPN-38 will not operate so it appears the reset circuit will operate at temperatures that the timer operates at:

The #2 FPN-41 timing cabinet chassis was completed, wired in & tested - operation appears normal - cont. on with assembly of the 100KC amplifier circuit - it must be tested out before assembly in the chassis -

7/18/62: Received letter revising FPN-38 completion date to 1 Sept 1962:

Applied a negative pre-set to the "K & L" divider (1x0) board (as modified) at the time of timer manual

W-234 (CONT)

7/18/62 (CONT). reset and adjusted the proper (in synch with the divider) 1/2 P.R.R. waveform upon each reset — this incorporated into the reset circuitry and construction of the remaining reset circuitry on the chassis is continuing:

Preparing engineering model of chassis 100KC amplifier for tests, adjustment, etc

7/19/62 Construction of the engineering model of the FPN-38 continuing — all parts probably will fit on the 4 boards attached to the divider holder:

Looking into the FPN-41 reset/timing chassis to determine the stability of the "timing pulse" being generated from the clock info —

7/20/62: Const. of FPN-38 chassis continuing — should be done today —

Set up a delayed clock trigger thru the hp time computer in order to accurately check the stability of the FPN-41 generated timing trigger — find that the presently installed delay phantastron is unacceptable as pulse jitter and jump runs out to greater than 60 usec — will have to improve or find new phantastron or find some other means to delay the trigger by ~1000 usec.

7/23/62: Setting up the completed FPN-38 divider/reset chassis for test — found some difficulty with poor connections on the 4215 plug-ins — corrected — having trouble getting the gating FF to operate properly and produce the desired output level for the diode gate — the 1214 FF has a tendency to stay in the on (high) state and not turn off with the + signal coming thru the pulse transformer — this is function of the push-button trigger generator loading and the pulse amplitude & signal coming from the pulse transformer — plan to re-design the transistor amplifier ahead of the pulse transformer to give more signal (increase size of the collector by-pass capacitor) and work on improving the loading on the 2N1214 base from the push button output circuitry —

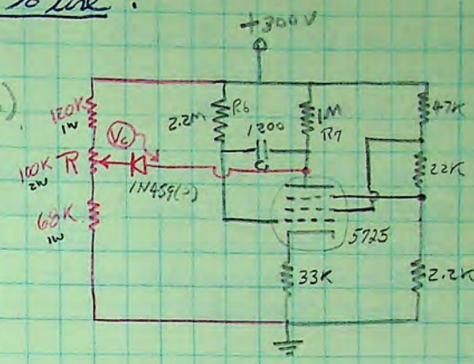
On the FPN-41 delay phantastron circuit — plan to change this so that the output square waveform delay is a function of a holding voltage (clamp level) on the plate rather than control the delay by varying the value of the grid resistance —

W-234 (CONT)

7-24-62:

RN/FPN-41 delay phantastron to use:

t_d = OUTPUT DURATION $\cong R_6 C_1 \frac{V_c}{E_{bb}}$ (sec)



desire to have a variable delay of from 500–1200 usec by adjusting R

using values as shown

① $R_6 = 2.2M$ $C_1 = 1200 pf$

$$V_{c_1} = \frac{t_d (E_{bb})}{R_6 C_1} = \frac{(1200 \times 10^{-6})(300)}{(2.2 \times 10^{-6})(1200 \times 10^{-12})} = \frac{300}{2.2} = \underline{\underline{136 \text{ VOLTS}}}$$

$$V_{c_2} = \frac{(500 \times 10^{-6})(300)}{(2.2 \times 10^{-6})(1200 \times 10^{-12})} = \frac{500}{4(2.2)} = \underline{\underline{56 \text{ VOLTS}}}$$

② $R_6 = 2.2M$ $C_1 = 1000 pf$

$$V_{c_1} = \frac{(1200 \times 10^{-6})(300)}{(2.2 \times 10^{-6})(1000 \times 10^{-12})} = \frac{3600}{22} = \underline{\underline{164 \text{ VOLTS}}}$$

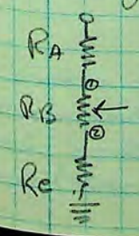
$$V_{c_2} = \frac{(500)(300)}{(2.2)(1000)} = \frac{300}{4.4} = \underline{\underline{68 \text{ VOLTS}}}$$

③ $R_6 = 1M$ $C_1 = 1000 pf$

$$V_{c_1} = \frac{(1200)(300)}{(1)(1000)} = \frac{3600}{10} = 360 \text{ VOLTS} \leftarrow \text{NG}$$

Looks like ① or ② above will do:

∴ per using ② above to keep C_1 as small as can



$R_A = 120K$
$R_B = 100K$
$R_C = \frac{68K}{288K}$

$I = 300/288K = 1.04$ ma

drop across $R_A = (1.04)(120) = 125V$
∴ appearing at ① = 300 − 125 = 175 V ✓ OK

drop across $R_B = (1.04)(100) = 104V$
∴ appearing at ② = 175 − 104 = 71 V ✓ OK

$R_6 C_1$ ±5%

jitter should be < 0.1% or < 1 usec on < 1000 usec delay.

W-234 (CONT)

7/24/62 (CONT): Checking divider for resistor power dissipation:

125
104
229

$P_A = (125)(1.04\times10^{-3}) = .135$ watts (∴ 1W OK)
$P_B = (104)(\ \ ''\ \ ) = .114$ " (")
$P_C = (71)(1.04\times10^{-3}) = .074$ " (")

300
229
71
229
-20

In testing modified circuits (changed value of transistor bypass caps in 2N1303 to .01 μf) shorted out parts of circuit due to wire having lodged across transistor F.F. (INHIBIT 2N1214) — corrected this — replaced 2N1214 — 2N1303 still bad — to complete & test tomorrow.

7/25/62 Cont. working on the FPN-38 reset/timing circuit — varying the component values in the push button reset circuit to decrease its loading effects on the gating flip-flop (2N1214) — circuit operating OK —

7/26/62: Tested the FPN-38 timing/reset circuit external to timer and operation appears normal — commenced installing the circuits and hooking into the FPN-38 — keeping record of detailed installation to form basic installation instructions —

7/27/62: Continuing to install reset circuitry into FPN-38 timer — putting in a small DPDT switch for facilitating complete disconnection of the divider inhibit and the K divider preset.

7/30/62: Completed basic installation of the FPN-38 timer timing/reset circuitry and initial tests indicate operation satisfactory — although some cleaning up will be necessary on the methods of coupling in the inhibit waveform from Q_{11} — also the cable used to run from the timing/reset circuitry (presently using a good quality shielded cable as used by Sperry in the FPN-38) must be investigated.

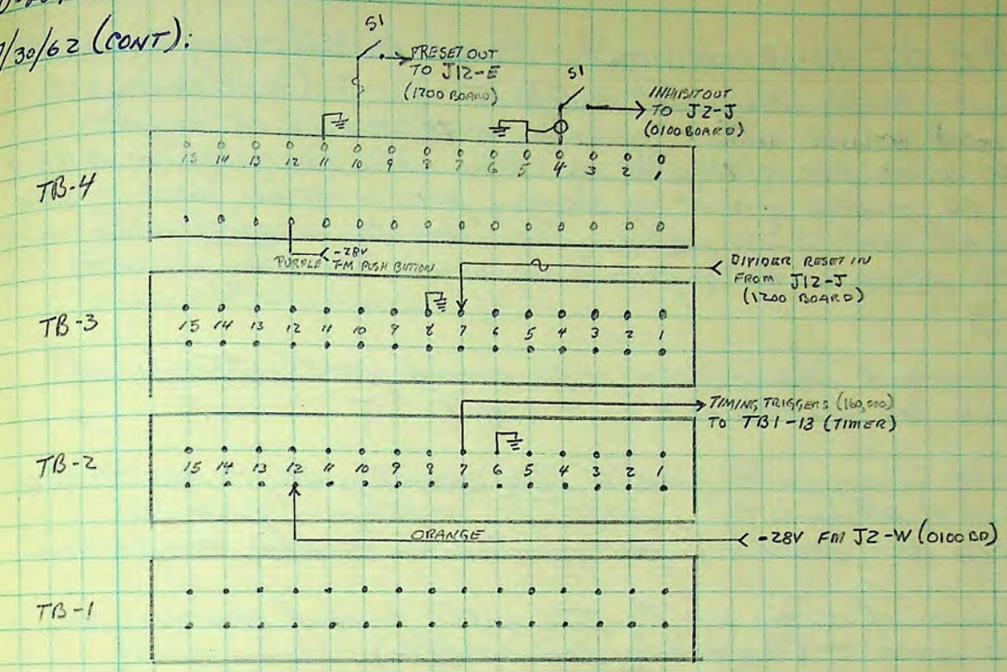
Completed running the monitor/reset functions from the timer to the timing cabinet (monitor & IRIG selection panel) — all functions appear normal with no apparent loading on the timer circuits.

Commenced building the second FPN-38 chassis as done in the first model.

The following data lists key circuit connections made to the FPN-38 timer for picking up power and timer info to run the reset circuit; for inserting the necessary timer inhibit and K divider pre-set (to insure proper ∅ code on each reset) and for picking off monitor information —

W-234 (CONT)

7/30/62 (CONT):



W-234 (CONT)

7/31/62: Cont to test FPN-38 reset circuit – changed the cable carrying the inhibit waveform from the timing/reset circuit to J2-J (0100 BOARD) to micro-dot coaxial cable – operation of the circuit OK. – get positive reset back to time of 1a time and can adjust ± 3 to 5 usec the position of reset by changing phase of 1KC in clock – also get reset back to the same phase code upon each reset – (ie the same ½ PRR sequence as is in the timing/reset circuitry):

Commenced chasing down parts needed for the two fenal chassis for the FPN-38 reset circuit –

8/1/62: FPN-38 timing/reset circuit still operating OK – must allow about 15 to 20 minutes warm up of timer (from a completly OFF condition) for positive reset back to zero on time.

Commenced wiring up the two addl finished chassis for FPN-38 reset – (work being done in lab-)

8/2/62: FPN-38 timing/reset circuit still working – approx 0.2 usec jitter may be seen observed between divider used and the generated 160,000 usec timing pulse.

Checking on order for four addl DEC-4215 Boards – called Pennsylvania – order should be here by end of August for shipment.

Commenced putting together a complete spare parts list for the FPN-38 reset/timing circuitry –

8/3/62: FPN-38 timing/reset circuit still working – starting on the installation and operating instr.

Working on the alarm system – some difficulties encountered since the time ½ PRR waveform is so sloppy and slow rising –

Const of the two finished chassis cont.

8/6/62: FPN-38 timing/reset circuit still working – reset worked immed on energizing the timer today –

Still working on an acceptable alarm circuit – const. of the two finished units continuing –

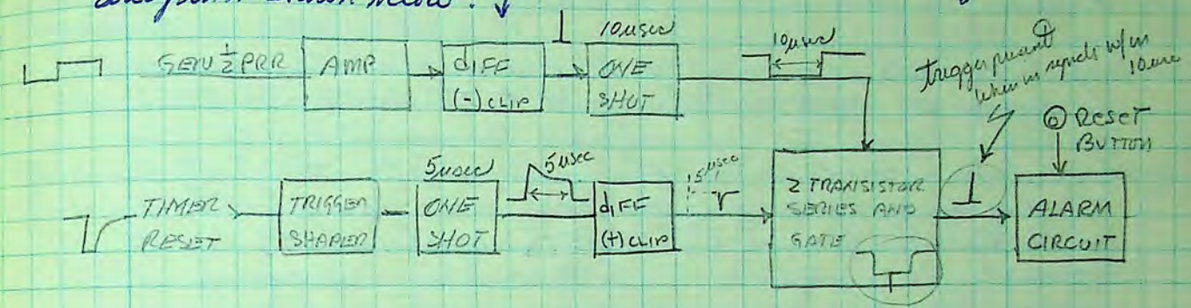
8/7/62: FPN-38 timing/reset circuit still working OK – still working on breadboard of the alarm circuit – construction of the two finished units is continuing – scope (topsy) in FPN-38 timing

W-234 (CONT)

8/7/62 (CONT):

cabinet failed this date due to excessive heat – taking scope out and setting up plans to move the blower from the bottom to the middle of the timing cabinet –

8/8/62: FPN-38 reset circuit working OK – cont. w/ const. of two fenal chassis – cont. to investigate an alarm circuit following the diagram shown below: ↓



Picking up odds & ends on timing cabinet (FPN-38) – starting on writing installation instr – routing cables – etc

8/9/62: FPN-38 reset still oper OK – two Boards finished up late today – ready for mounting harness wiring – ordered a large capacity axial exhaust fan to mount on top of FPN-38 timing cabinet

Drawings to A.E. on reset schematic – took scope pictures – laying out repair write up – cont with monitor installation –

8/10/62: Removed FPN-38 reset circuit from synchronizer to get wiring set up for two new finished boards – circuit operated OK & o/o failure since 7/31/62 & ie 10 days

Wiring up new boards – making cables – making cable drawings – writing repair & setting up drawings, photos needed – etc.

8/13/62: Received exhaust fan for FPN-38 timing cabinet & preparing installation – cont. w/ wiring of new chassis (divider & reset) leads – rec'd panels from WRS

8/14/62 Cont. w/ mounting fan – new panels – wiring in timing cabinet – installed #2 divider & reset chassis – followed & corrected installation instr – tested chassis as installed and it worked OK except that got about 30 to 40 usec offset in time of 160,000 usec trigger & ensuring divider resets – investigating this –

W-234 (CONT)

8/15/62: Continuing with testing of the #2 FPN-38 "Divider & Reset" Chassis (timing modification) - all the new circuitry appears to operate OK but still getting a time diffrence between time of divider reset and the time of the 160,000 usec clock pulse after push to reset - the divider reset appears on the trace earlier than the 160,000 usec pulse so when the 100KC square is inhibited, it appears that the FPN-38 timer divider chain is continuing to run long enough (after the 100KC is stopped) to cause the timer divider to be set mad on zero but at some point along early in the count - measured the amplitude of the 100KC input to timer (from osc) & the URQ-11 & 0200 input amplitudes are appear the SAME - Then went to the AN/FPN-38 technical Manual, Volume I and adjusted the amplitude of the 100KC signal on Z5-14 in the transmitter adaptor to exactly 5V peak to peak using R109 in accordance with paragraph 2-9-g (3) of the technical Manual, CS-273-59 (see page 2-34) - this cleared up the problem and there is no discrepancy now between the time of normal divider resets and the 160,000 usec clock pulse which ensue after push to reset -

Therefore, it appears that the 100KC square (Q3 & Q4 on the 0300 Board in the timer) is sensitive to the amplitude of the input 100KC on the base of Q3 (where we are also inhibiting to cause timer reset to the clock) and if the amplitude is too great the 100KC square will continue to operate for a short time AFTER the 100KC is stopped giving the discrepancy noted above

Now plan to investigate:

① the ranges in 100KC amplitude adjustment of R109 to give satisfactory timer reset

② addition of decoupling resistance between the coupled emitters of Q3 & Q4 in the 0300 board in the attempt to reduce any positive feedback sufficiently to allow a greater range in the variation of the input 100KC signal to the 100KC square - and thus a desired timer reset each time even tho R109 may not be adjusted exactly as specified.

Continuing with run in test of #2 divider and reset Chassis and with final assembly of the timing cabinet and #1 divider and reset Chassis - mounting del name tags - etc

W-234 (CONT)

8/15/62 (CONT).

Modified one 0200 Board by installing a 12 ohm resistor in the common emitter lead between Q3 & Q4 in hopes of cutting down any regeneration in the 100KC square - tested by varying 100KC drive to timer from oscillator (at R109) and found that this corrected the variation in time between divider reset and the 160,000 usec trigger - w/o this emitter dc coupling resistance, could only vary 100KC drive a 0.1 of a volt or so above the estab 5V p.p. but after adding resistance, could decrease 100KC to 4.0V p.p and raise as high as 10V-p.p. and still get the desired timer reset - plan to confirm test on cold timer - had timer problems today - in -12V power to the dividers - investigating:

8/16/62. Cont. to check out FPN-38 timer to find reason for failure - finally found dirt, solder, etc in the plug in for the 5500 board - found most of the B dividers bad - replaced several transistors in the A & C dividers - resoldered one broken lead and timer was restored to normal operation - reset circuit mod operation still OK (#2 unit)

Made operational test of the reset system - put FPN-39 on SLO into dummy load - put FPN-41 timer in operation as slave station - jumped the FPN-38 and master signals (from FPN-38) came exactly back on scope where they should have been upon reset and in the proper phase code - - all operations checked out O.K.

Completed installation of timing cabinet ~~unit~~ xcept for small items - hooked into timer - operation all OK - started calling up some spares to ship out w/ the equipment - preparing for photos & installation of #1 unit for test - writing report - installation instr.

8/17/62. Photographs taken today - installed new #1 Divider & Reset Chassis for the modification - operation OK - performed an operational check on the system as done on 8/16 using FPN-41 as slave - check OK - resynch w/in same tolerance as timing equipment (ie w/in 0.2 usec) - Writing report - ops & installation instr.

8/20 & 8/21/62: Continuing to test DIVIDER & RESET CHASSIS #1 - operation still OK - making final adjustments - tagging - preparing to ship modification out on 22 August - writing installation instr and report -

8/22/62: Both HP-1601B scopes sent to lab for complete check out - installed a P2 CRT (5AM-P2) in one of the scopes - both operate OK

W-234/P CONT:

8/22/62 (CONT): Checked P-2 tube and presentation of "DIVIDER RESET" & "160,000 usec timing pulse" together seems much better — took out DIVIDER & RESET CHASSIS #1 — operation OK — both #1 & #2 units tested OK & ready to ship out.

Completed bread board model of the Timing Modification Alarm Circuit — alarm will sound when ever the timer becomes out of step with the clock by more than 5 usec either way — this device could be utilized to automatically reset the timer on a pump — going ahead and ordering parts for construction of an engineering model —

8/23/62: Reinstalling the engineering model of the DIVIDER & RESET CHASSIS into the FPN-38 getting ready to disassemble timing cabinet and packaging modification for shipment to FAROES (FAERØNEA) — cont. w/ writing of installation instr (Annex B) — operating instr (Annex A) & Report I

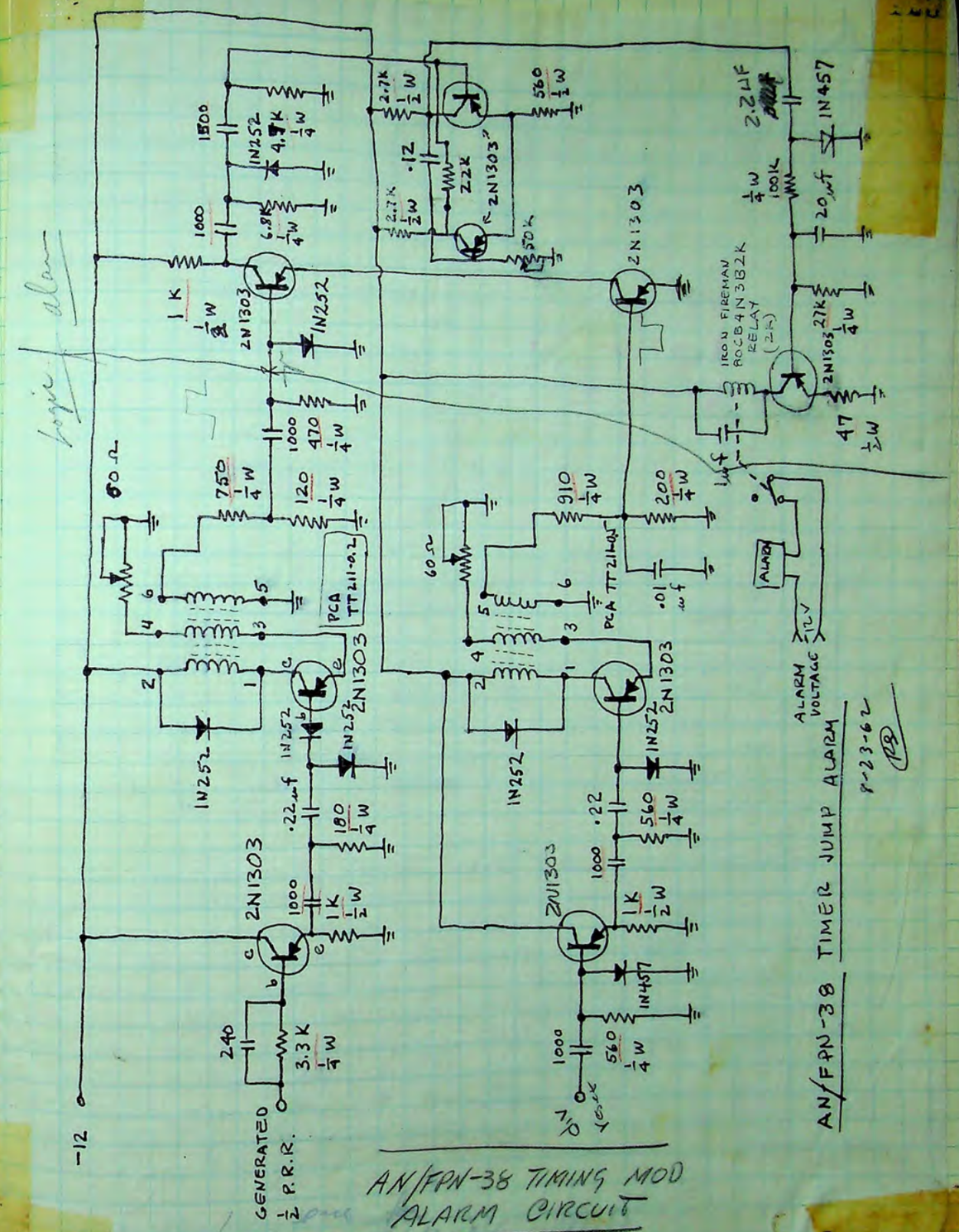
8/24/62 Packaged AN/FPN-38 TIMING MOD for shipment to FAROES — writing on report — installation instr & oper instr.

Went back to AN/FPN-41 phase of the project and commenced to finish up wiring of 100KC amps into chassis — will perform mod to delay phase to make more stable —

Schematic on adjacent page is of the alarm circuit for the FPN-38 Timing Modification: — parts are on order —

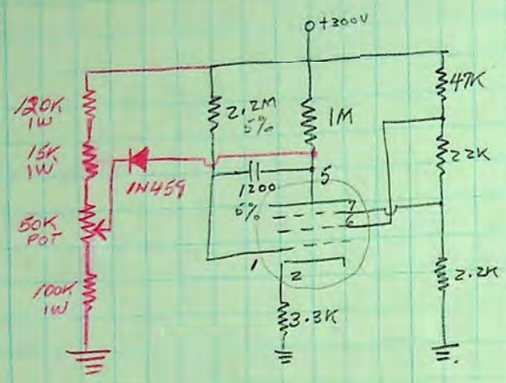
8/27/62: AN/FPN-38 Timing Modification shipped to Brooklyn today — cont. to write report — installation & oper instructions.

Discussed an alarm circuit to detect when the two clocks (& D&R dividers) are not tracking — plan to have this alarm mounted in the timing cabinet and to be in the form of a LIGHT which will remain lighted as long as both clocks and both Divider & Reset Boards are tracking together — then if the other alarms (ie timers tracking on the clock) sound, it can be determined at a glance if the out of track alarm was caused by a timer jump or caused by a clock (and associated Divider Reset Chassis) jump —



W-234 (CONT)

8/28/62: Returned to the FPN-41 Timing Modification – performed a change to the delay phandistron circuit to allow delay to be controlled by a voltage in lieu of by a potentiometer in the grid lead – to increase stability –



achieves stable (w/in 1 μsec) delays

range 800 to 1200 μsec

8/31/62 JRE

Discovered that in the 100KC amplifier circuit, the 2N1131 transistors have their collectors internally connected to the cases – this precludes using the already built board with the aluminum heat sinks connected to ground – will have to order (done) a different type of heat sink and completely rewire the amplifier using smaller terminals on a smaller, thinner board – layout being done and fiber terminal board material is being ordered.

8/29/62: Tested the modified FPN-41 timing drawer with the changed delay phandestron circuit – still experiencing pulse instability in the timing pulse – now suspect the Time Comparator (being used to get a delayed clock trigger) may be at fault – used timing pulse as a trigger and observed the FPN-41 divider reset pulse for jitter – RESULTS: jitter appears now to be less than 0.5 μsec and there were no jumps observed (as before) – going ahead with this circuit. – setting up plans to have Lab Inst. Mechanic check operation of the time comparators:

Control on delay phand too wide with the 100K pot installed above – made measurements of resistance needed for delay control from 800 to 1200 microseconds

W-234 (CONT)

8/29/62 (CONT):

and found that need only 50K control – ∴ changed the voltage divider by adding 15K to upper (nearest +300V) resistor and changed lower one to 100K

Tested above mod – used gen timing trigger to trigger scope and monitored drift in divider reset circuit with K env servo disengaged – drift now ≈ 1 μsec and about 2 max – this considered acceptable – will modify second set up and test

8/30/62: Modified & tested second delay phand. change – OK – get same approx drift as above:

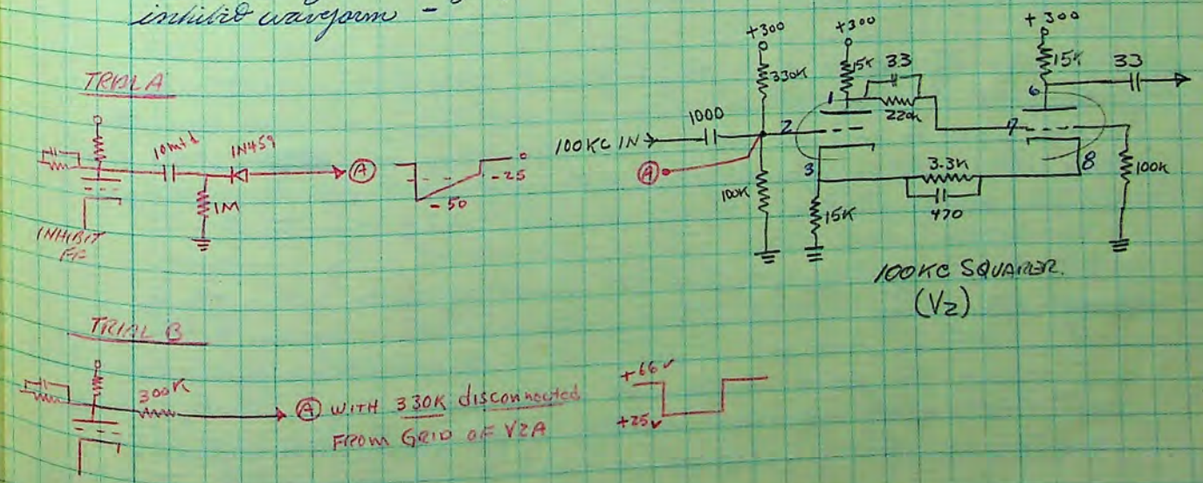
8/31/62: Tested LSTS mixer circuit & all appears OK – setting up for testing the reset system – some instability experienced in the inhibit F.F. – Checking out

Made up order for FPN-38 timing modification spare parts to be shipped later to FARCES – cont writing report – operint for FPN-38 timing mod.

9/4/62: FPN-41 timing problems – trouble shooting – ready to attempt to inject an inhibit waveform into the timer divider at the 100 kc squarer –

Working on the FPN-38 clock alarm (2nd alarm) to detect when the two clocks are not tracking – writing report – etc

9/5/62: FPN-41 timing: setting up to go into the 100KC squarer with an inhibit waveform –

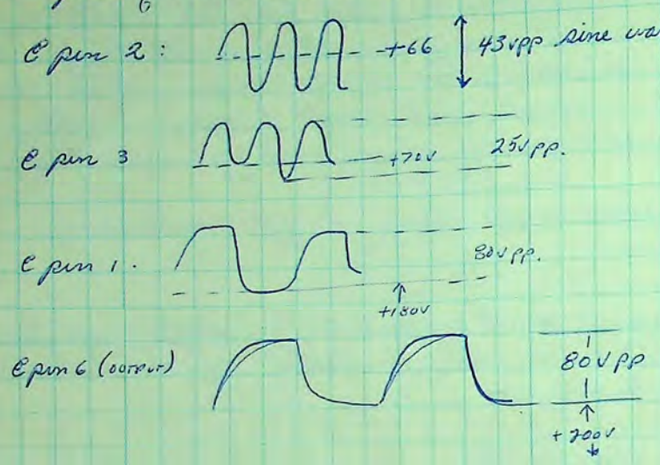


W-234 (CONT)

9/5/62: FIN-41 (CONT): Using method of trial (A):

VTVM

grid of V2A (100KC SQ) is normally at +66 vdc – cathode at +80 vdc –



Connected as per trial A and achieved fairly consistent timer resets but with approx 300 usec offset.

9/6/62: Investigated offset in timer reset described above – this offset is a delay type offset indicating that after the timer is un-inhibited, there is about 300 usec someplace before the divider gets going again – ensuing timer reset pulses occure AFTER the timing (1 sec) pulse – also this offset is consistent only if wait a second or so between pushes of the reset button – the 10 mfd cap does not completly discharge in repeated fast pushing of the button and thus the inhibit waveform on the grid is reduced in amplitude each time button is pushed unless you wait for discharge time –

Checked the 100KC BST tanged 9 and tanged 0 outputs in time with respect to the inhibit waveform – and do get some variations (10 – 30 usec or so) in time there depending on how fast the reset button is repeatedly pushed – if wait one sec or longer between button pushes, timing becomes fairly constant.

Checked to make sure that the 100KC squares is actually turning off at the start of the inhibit waveform (it is) and is turning back on at the end of the inhibit waveform (and does) BUT again if push button too many times in a short period of time, the 100KC square starting is OK but there are some variations in time as speed up rate of pushing button –

W-234 (CONT)

9/6/62 (CONT) It is apparent now that capacitor coupling in the inhibit waveform probably will not work and will have to try trial B

Still looking for 200 usec or so – looked at the trigger to the 10KC BST Driver in time with the inhibit waveform and they appear to start right up again – BUT looking at the 10KC BST Driver output, the switching waveform do exhibit delays up to 200 to 300 usec after the end of the inhibit waveform and the variation appears to be somewhat dependent upon the rate of reset button pushing – in the output waveform of the 10KC BST driver you can see small indentations where the driving triggers have had some influence but the F.F. will not flip on the first or second driving trigger and then takes off (usually) with the third driving trigger.

Going now to the inhibit methode of trial B in order to attempt stabilization of the errors found with the square and the 100KC BST – then will come back to the 10KC BST circuits and see if can find problems –

9/7/62: By increasing the size of the cathode bypass capacitor in the 10KC BST driver from 4700 to 0.1 mfd (actually effect is apparent when going to 0.05 mfd) can get one more good trigger thru to the F.F. and then get a discrepancy of only 100 to 200 usec

FIN-41 100KC BST DRIVER CHANGE

Then changed the value of C_{14} coupling the trigger from T9 of the 100 KC BST from 100 pf to 200 pf and this caused the first trigger of the line to flip the 10KC BST driver – note all the above done using method of TRIAL B with about 200 to 300K resistor in series between inhibit FF & input to 100kc squarer – reset discrepancy now only 30 to 80 usec and is due to the method of inhibiting the 100KC squares –

Changed the commutating capacitors in the INHIBIT FF from 22 pf to 330 + 22 = 352 pf each and this gave an inhibit waveform of a more steep nature with some overshoot – now the 100kc square turns OFF exactly at the time of reset and starts again exactly at the time of the un-inhibiting waveform

RESULTS: Success: get no discrepancy between the timing pulses and ensuing divider reset pulses –

W-234 (CONT)

9/7/62 (CONT): Now must go back and clean up the changes made — analyze the effects on circuitry and start construction of the engineering models:

9/10/62: Still looking at the FPN-41 100KC squarer and the inhibit waveform input circuits to determine optimum values of coupling resistance — get the same effect with the FPN-41 as did with the FPN-38 in that when equipment is first turned on, the timer will not reset to zero (with 235K series resistance coupling in the inhibit waveform) but it works OK after warm up —

Wired in the new 100KC amplifier in the timing cabinet drawer — ready for testing.

9/11/62: Worked on the inhibit circuitry again —

Tested the 100KC amplifier & measured harmonics in the timer w/ and w/o the 100KC going thru the amplifier — data as per sheet below:

	DB	Amp out	V103 cath FPN-41 w/amp	V103 cath less amp
~~OSCILLATOR~~ 100KC	0	0	0	0
200 KC	-32	-27	-27	-26
300 KC	-37	-35	-35	-35
400 KC	-62	-47	-47	-46
500 KC	-46	-52	-67	-67
~~600 KC~~	~~-62~~			

Looks like the amplifier is not introducing any additional harmonics — letting it run for test

W-234 (CONT)

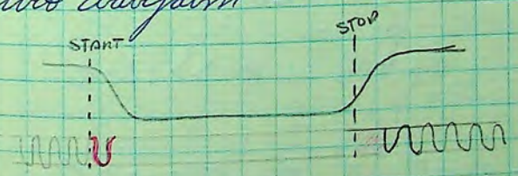
9/11/62 (CONT):

Found that FPN-41 will not reset the same using the timing trigger formed without the delay phantastron (ie, undelayed timing trigger) as it will with the delayed trigger — must check this out — apparently has to do with the shape of the timing pulse and its effect on the inhibit waveform — also want to investigate the FPN-41 100KC squarer circuit to see if can make it less sensitive to changes to 100KC on the grid —

9/12/62: Still working on FPN-41 reset — find that the shape of the timing trigger does have some influence on the shape of the inhibit waveform BUT this not critical enough to cause delays — the real problem of the delay in reset reported above is due to the delay thru the delay phantastron and schmitt shaper circuits as compared to delay with the one second clock pulse applied directly to the blocking oscillator — ie if the clock time reference is readjusted, the same reset can be experienced with the delay phantastron, schmitt shaper circuit as with the B.O. direct and the delay thru these circuits cause a phase reference difference between the 100KC in the timer and the 1KC in the clock —

Still getting a slightly unstable resetting of the FPN-41 timer depending on the adjustment (critical) of the size of the resistance coupling in the inhibit waveform — checking out

9/13/62: Checked the output of the 100KC squarer (in timer) to the inhibit waveform —



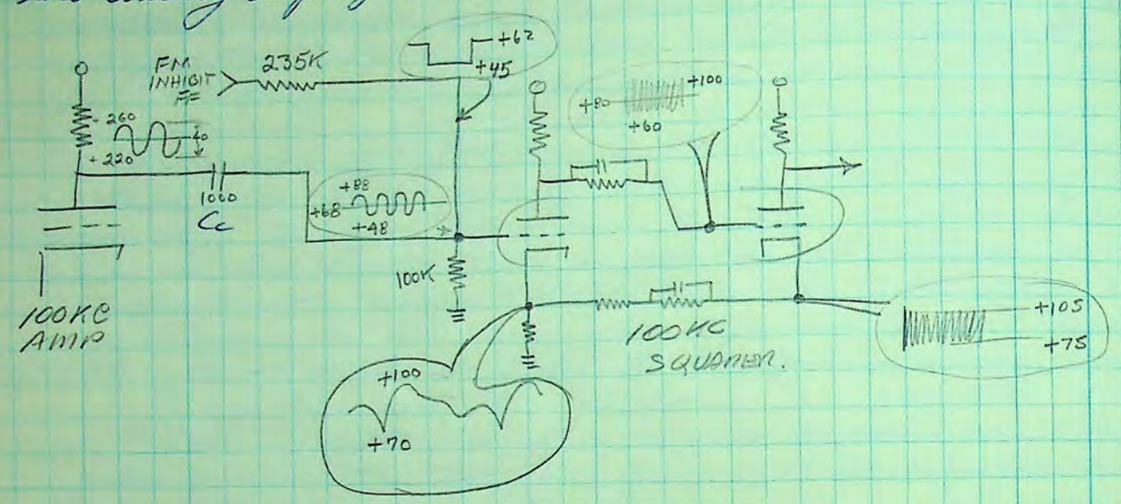
can see that we are not inhibiting exactly right — ie square wave output is going on after the start of the inhibit waveform and not starting until after the end of the inhibit waveform — apparently when we get a satisfactory inhibit, the two discrepancies cancel out — this is no good

The rise and decay time of the inhibit waveform is very poor when connected into the 100KC squarer as done in TABLE B of page 125 — tests show that this is not due

W-234 (cont'd)

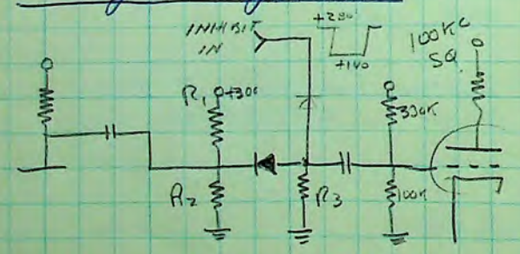
9/13/62 (CONT):

entirely to the size of the DC coupling resistances (ie maybe one or two usec are from this) - the real problem (giving 60 to 100 usec change in rise and decay times) appears to be the circuitry coupling in the 100KC to the squarer.



Must isolate the 100KC amp to get good sharp inhibit - cannot increase size of Cc as this would cut down 100KC amplitude too much -

Will try something like this



R_1 = 100's of K

R_2 = MEGS

R_3 = MEGS

$R_2 + R_3$ in ‖ >> 100K

Put a badly distorted 100KC signal into the FPN-41 timer to test degree of filtering of the 100KC amps - Ran spectrum analyzer:

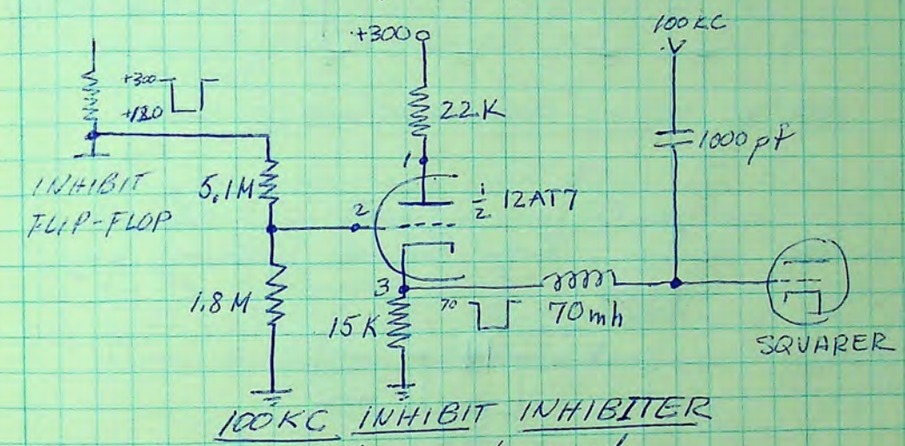
f	100KC INTO TIMER	100KC at V103 (output) pin 3 cathode		
100 hc	0	0		
200 hc	- 26 db	-60 db	Δ	- 34 db
300 hc	- 48 db	-50 db	Δ	- 2 db
400 hc	- 60 db	—— (NIL)		NIL
500 hc	- 85 db	—— (NIL)		NIL

∴ 100KC filtering pretty good.

W-234

9/14/62 FPN-38 timing mod OPERATING INST (appendix A) sent to TAC for review: - timing mod Interim Report No 1 started thru 0-3 for initial review before sending to TAC - INSTALLATION INST (appendix B) masters have been corrected and ready for reproduction - figures for all three sections are not ready for reproduction.

4-17-62 AN/FPN-41 the inhibit waveform was coupled in the divider using the following circuit



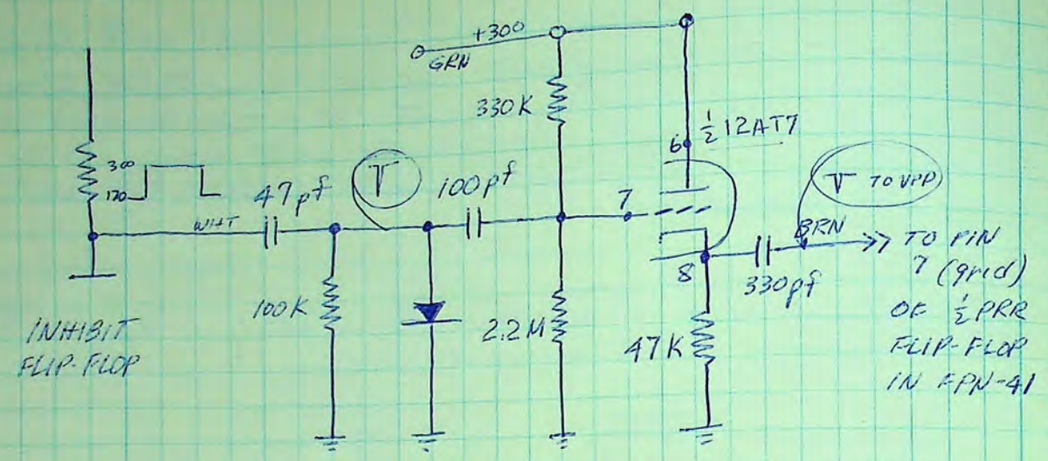
a uniform reset was observed

9-18-62 AN/FPN-41

A preset trigger was developed from the "other half" (plate that is Normally conducting) of the inhibit Flip-Flop and coupled through an cathode emitter follower, (other half of the 12AT7 used for INHIBIT) to pin 7 of the ½ PRR flip-flop in the timer

Tests show that the timer resets in the proper phase code, using this preset trigger.

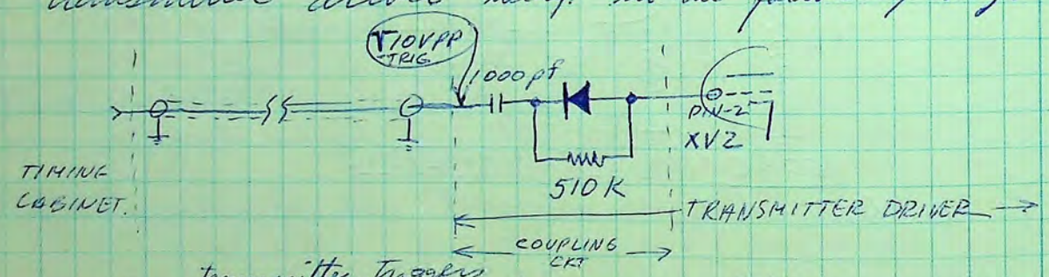
See other side for Preset Generator schematic. (Page 132)



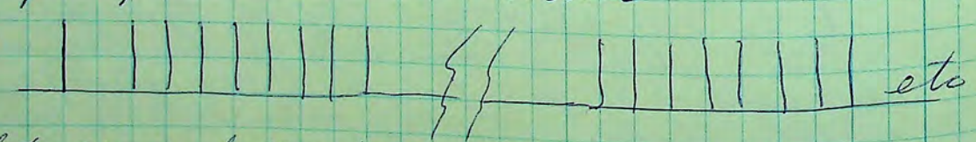
FPN-41 PRESET GENERATOR AND COUPLER

9-19-62

The 1 second pulse was injected in the transmitter driver today. in the following way:



the 8 ~~pulses~~ transmitter triggers with the 1 second ~~pulse~~ triggers 2000 μS before 1st ~~pulse~~ trigger were observed at the output of the transmitter driver

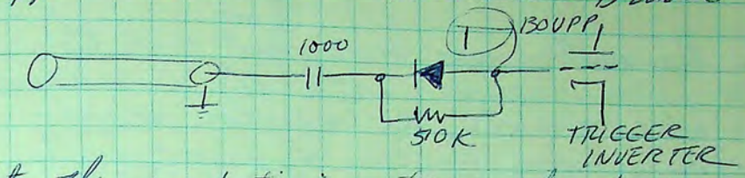


Had to secure at 1300 for W-

This method of Timing trigger injection allows the timing puls to be varied in 10 μ Sec intervals — we don't want this.

9-20-62

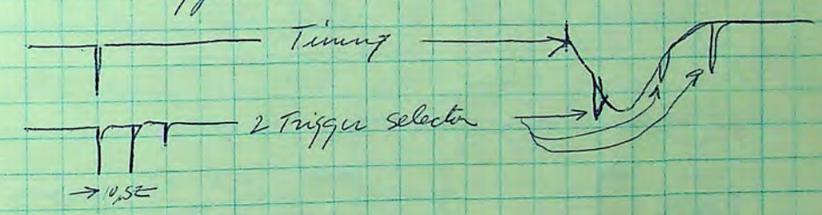
the timing pulse was injected on grid of trigger inverter in Transmitter Driver chassis.



Note the input timing trigger has to be adjusted at same amplitude (130 VPP) as the selected triggers. the selected triggers are viewed on CRO as a group of 2 or 3 triggers 10 μS apart (2 trigger selector gate output

The Timing pulse was set 2000 μS before Master interval (MZ interval) in this manner:

1.) On an ~~expanded~~ fast sweep align the timing pulse with the first selected trigger of the group from 2-trigger selector



Note

the Transmitter triggers cannot be used for this alignment because of the characteristics of the Thyratron.

2.) Note the Time Difference reading on the HP clock, Subtract 2000 from that number and set the dial for that number. the timing pulse is now 2000 μS befor the multipulse group

example

TD reading with trigger (1) 918854
Subtract 2000
set dial for 916854

9-20-62 (cont)

TILT

The transmitter was energized and the radiated pulse groups with the 1 second pulse were viewed on monitor scopes

[A DRIFT BETWEEN THE STD. 1 SEC PULSE AND THE PULSE GROUP WAS OBSERVED]

this effect will be investigated

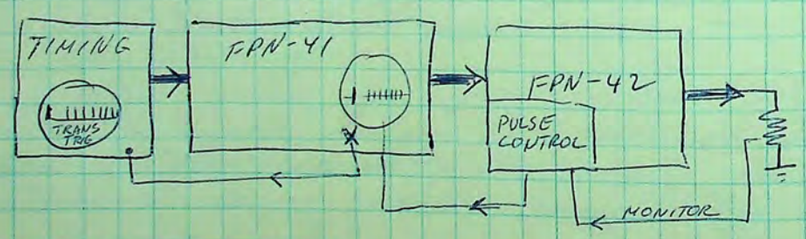
approx 1000μS / 20 min ??

OK now! the M Cycle servo was energized.

ew?

9-21-62

The FPN-41/42 equipments were energized in dummy load to check the performance of the STD. Time Transmissions.



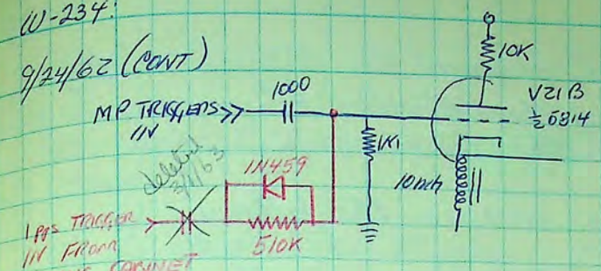
A stable transmission was observed.

LOOKS GOOD! PS

9/24/62 Cont'd with injecting XMTR trigger — and the one second trigger in on the grid (pin 7) of the M.P. trigger C.F. (V-21B) in the delay chassis using the coupling circuit shown on the next page →.

W-234:

9/24/62 (CONT)

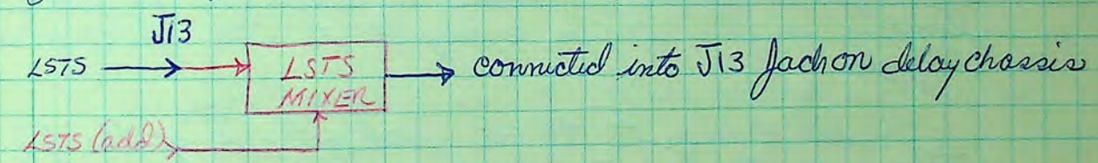


coupling circuit for inserting the 1 PPS trigger into the multipulse line (delay chassis)

trigger goes in OK but not occuring 2000 usec ahead of the first master pulse — below int Y internal and selecting XMTR to accuracy of 50KC with Y-50KC — NG — Checking out

Checked operation of timer inhibit & reset — still operates OK — checked LSTS mixer and it is still operating OK —

9/25/62: Coupled in the LSTS (add) waveform into timer at J13 of the delay chassis:



The LSTS mixer isolates LSTS add from MTS OK!! — Checked modified LSTS at LSTS gate in delay chassis and looks OK:

Checked method of trigger insertion done 9/24 and with the Z delay set out past 50,000 (as it normally is) we get selection of the one second trigger from Y internal 50kc and this is unacceptable — investigating to see if can bring Z delay in & use Z internal 50KC to get desired trigger selection & then vary Z ext servo to get desired positioning !!!

Cleaned up wiring runs — started fabrication of the chassis to go into the divider drawer and to hold all used circuitry except LSTS mixer —

9/26/62: Checked FPN-41 circuit diagrams and decided that above method of inserting the 1 pps trigger is valid — ie if can set the Z delay switch just right, can provide Z internal 50KC for proper selection of the 1 PPS trigger —

9/24/62: Set the Z delay at 48800 and observed the trigger existing during the last 1200 usec of the interval (Z INHIBIT OFF) - this still NG - selecting in the 1 interval

Set Z delay at 48000 - now can see the following —

① With Z inhibit switch ON see only the 1 pps trigger occuring & can position it in 10 usec steps (over range of 20 usec) to be exactly 2000 usec ahead of the first master group by turning the Z env-servo - this trigger is stable (ie @ 49,000 usec)

② With Z inhibit switch OFF see a Z trigger at 48,000 & at 49,000 - the 49,000 usec trigger is coincident with the 1 pps trigger and the LSTS add part of the modified LSTS permits only this one 49,000 trigger to come thru once each second - But the Z servo drives (on noise ?) and get 10 usec jumping of this trigger w/respect to the first master trigger

③ Set Z delay to 48,010 and get rid of the 48,000 trigger - turned Z inhibit switch OFF and got a stable 1 pps trigger - monitored for over two hours and it remained stable — all looks OK here

As of this date can effectively accomplish all the project requirements listed below

① Can repeatedly reset in time to the clock w/in much less than 1 usec

② Can insert the LSTS (add) waveform into the time LSTS line w/o adverse effects -

③ Can satisfactorily insert the 1 pps transmitter trigger exactly 2000 usec ahead of the first master pulse (± less than 0.5 usec)

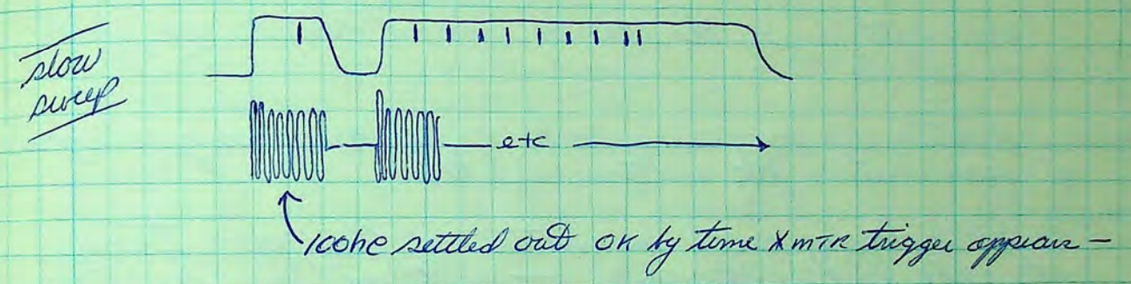
Proceeding to connect up the 1 pps trigger coupling components on spare terminals of a terminal board.

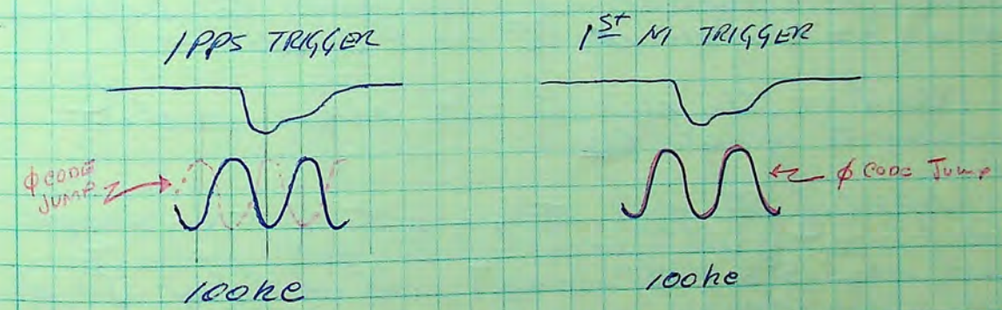
9/26/62 (CONT)

near V21 (delay chassis) — continuing with fabrication of the hinged chassis to hold all the basic reset circuitry —

① Checked XMTR triggers - trigger w/ positive rise of LSTS add — see 1 pps trigger inside LSTS add OK — also M & pulses inside LSTS OK —

② Checked LSTS (modified) & 100kc to XMTR drive —





the φ of the 1 pps 100kc is same as first M 100kc at the time of the trigger on reset and upon each reset — the trigger look the same & 100kc looks the same — all looks OK

③ delay between 1 pps trigger & the 1 pps pulse entering the timer is about 15 usec - this is OK since 1 pps XMTR trigger is exactly 2000 usec ahead of 1ST M trigger —

9/27/62: Cont. with construction of the FN-41 reset chassis - assembling parts for second chassis - constructing circuit diagram - layout component designations - finished installing the 1 PPS trigger insertion network on existing T.B. of delay chassis

9/27/62 (CONT):

Set up the FPN-42 into dummy load and operated timer with the 1pps trigger for over two hours — reset timer repeatedly and all looks good — amplitude of the 1pps pulse (xmtr) is about the same amplitude as the first master pulse — no jitter — stable pulse exactly 2000 usec ahead of the first master pulse:

Will now layout LSTS mixer circuit on a small terminal board suitable for installing in the bottom of the delay chassis:

Work continuing on the FPN-38 alarm circuits as parts are received.

9/28/62: Writing up progress report — squaring away diags & schematics for installation rpt #1

Still playing with insertion of the 1pps trigger into the delay chassis — method is OK but could be troublesome if ever want to add a third or 2 slave in the coarse chassis —

Wired in the separate LSTS mixer and it appears to operate OK

10/1/62: Inserted the 1pps trigger into XMTR DRIVER chassis at grid (pin 2) of the gate generator and mix LSTS & LSTS (add) just ahead of J4 on XMTR driver chassis — get good stable pulse but it sits 2010 micro-seconds ahead of the first master on normal accurate (to time ϕ) reset —

Plan to contact Bartsen on this to see which method he wants — this system (above) permits independent insertion of the 1pps trigger (ie not dependent on Z interval information) but instead of being exactly 2000 usec ahead of the first master pulse it is 2010 usec ahead — checked phase of the 1pps 100kc at the trigger and compared to same done for master (first) pulse — get same results as shown on page 137 — still all looks OK

W-234 (CONT)

10/1/62: Checking on the FPN-41 timer +300V power supply to see exactly what its power capabilities are and to determine if the timing mod. circuits will cause too much loading (ie 125 ma during normal operation and 175 ma during reset) — also want to know to see if can also add on the Civil Defense timer contact circuitry (Mr Manning) —

Timing Mod Long on FPN-41 Power Supplies

est that total load on the +300V power supply by addition of timing mod is approx 150 ma and ±50 ma for pulsed loads.

The timer +300V power supply is rated @ 900 ma — Under normal operation, the timer only (plus some spare gear inserted here & there for spectrum improvement mod.) draws approx 700 ma from the +300V supply. With the timing modification connected, the steady (770 MS) drain on the 300V power supply is measured to be < 800 ma. During reset (push of button) the total load on the 300V power supply reduces to approx 750 ma. ∴ it is felt that the load does not exceed capabilities (continuous) of the timer +300V power supply —

10/2 → 10/11: Fabricating the FPN-41 reset chassis (2 ea) — installed one LSTS mixer into XMTR driver drawer — installed circuit for coupling in the 1pps trigger — HQ. Project Engineer stated on phone that he wants method used whereby the 1pps xmission appear exactly 2010 usec ahead of the first master pulse — Running remaining input/output cables between timer & timing cabinet — laid out final panel (timing cabinet) drawings & designated all cables — ordered front panels — rest of parts needed — commenced installing one reset chassis

10/12/62: Completed installation of first reset chassis — circuits seem to operate OK but get a delay in reset — ie ensuring divider reset pulses do not coincide with the timing pulses but are delayed approx 15 micro seconds — starting investigation — changing lead from chassis to squarer (INHIBIT) from single line to coaxial.

TIME COMPARATOR INVESTIGATION:

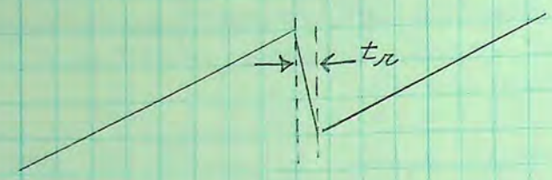
The HP time comparator sent to lab was aligned and tests showed the saw tooth horizontal sweep

W-234 (CONT)

10/12/62 (CONT)

output from the comparator is steady – the rise is quite linear and no jumping experienced

Looking at the saw tooth sweep (horizontal) output from time comparator & noting the neg. going (end of sweep) portion note following:



① In using the time comparator H output for a negative going delayed trigger to apply to scope for purposes of measuring the time of occurance of the 1pps XMTR (FPN-41) trigger, the t_r becomes important. ie want to know EXACTLY how many usec ahead of the first master trigger the 1pps trigger is occuring (should be 2000 or 2010 usec EXACTLY)

② In normal use of the time comparator for observing the WWV signals, the saw tooth rise is utilized and not the negative excursion. ∴ t_r not important for normal designed use of the comparator.

③ The t_r changes depending on the sweep rate selected with the comparator. ie on the 1000 msec sweep the t_r runs greater than 40 usec and on the faster 1 msec sweep the t_r reduces down to approx 2 usec. ∴ if use the 1000 msec sweep, the negative trigger used to 2 scope will tend to be unstable and this is the basic reason why the sweep of a scope will be unstable and will observe drift & jumps when using the comparator H output as a neg trigger –

④ The time comparator, properly aligned is accurate to within the meas. capability of the system – ie on the 1 msec sweep, full deflection (horiz) of the scope between lines is 1000 usec – each division is 100 usec and the intensity modulation dashes and spaces are 10 usec. The time comparator H output can

W-234 (CONT)

10/12/62 (CONT): be used to get a negative trigger (delayed in steps of 1000 usec) for application to the HP160B scope and it is possible to make time difference measurements between the 1pps & 1st master trigger of less than 1 usec – any drifting or jumping due to the unstable trigger is long term and does not influence these short term measurements.

This procedure will be recommended in the operating instructions (listing limitations) and the subsequent progress report will reflect time comparator findings with respect to the previously reported instability. –

FPN-41 RESET CIRCUIT:

Found reason for the installed reset chassis not operating properly – a commutating capacitor was left off the coupling resistor from the INHIBIT F.F. to the INHIBIT CATHODE FOLLOWER: – all functioning OK – cleaning up wiring –

10/15/62: Cont. to clean up Reset Chassis & other circuits incl. in 41 – taking data on all connection points and interconnections for installation instr. – preparing covers for scope amplifiers –

Returning to FPN-38 alarm circuits – parts (some more) have come in & plan to mount reset alarm & while waiting remaining parts – working on breadboard of alarm to detect two DC-421S divider units not tracking –

Took data on position of M cycle & shifter vs rotator position of 1pps trigger (2010 or 2000 usec) with fixed M trigger – later will have to determine exact phase relations for desired position but can't do now as FPN-41 being aligned –

TRIGGER DELAY	DIAL	TRIGGER DELAY	DIAL
2010	0	2000	5
2010	1	2000	6
2010	2	2010	7
2000	3	2010	8
2000	4	2010	9

Operating instr should reflect this as regard to position of the MC cycle & shifter and position of the 1pps trigger.

W 234 (CONT)

10/16 → 10/22/62: Breadboard of the second type alarm for the FPN-38 timing mod oper. OK — (to check tracking of the DEC Dividers #1 & #2 ie, to check clocks tracking) — now have to wait for relays & then test that phase

Parts dribbling in for the other alarms — still awaiting the relays & some small voltage capacitors (FPN-38 timing mod). — Contacted distributor of alarms & they are being sent on 10/24 (see phone call memo on 10/19/62)

Continuing with gathering data on installation & oper of FPN-41 timing mod for write up — making minor changes to 100KC amps to bring both them into identical appearance —

Tests performed on 100KC phase shifter by Colling — (see W-234 folder for precise data) — used new Ad V delay & phase comparator — NIELSEN & shifter package tests out as more accurate than the equipment used to measure its accuracy — found that can reset the micro-second dial to within 2 to 4 nano-second (.002 to .004 usec) and run out variations (w/insertion of continuous delay up to 1000 usec) shows max variation is 63 nanoseconds (.063 usec) at 1000 usec — This measurement is pushing the stated accuracy of the measuring equipment and in using an alternate methode to measure run out (p 3 in data) we that variations are sinusoidal out to 100 usec — Therefore, it is believed that the mechanical package accuracy falls well within the desired (project requirement) output accuracy of 0.02 to 0.05 usec since this implies small range accuracy & repeatability & must indicate this will be as good as or better than 4 to 7 nanosecond (.004 to .007 usec)

100KC Phase Shifter package last-time

Investigating a reset error in the FPN-38 timing mod (~10 usec from zero) which has appeared since re-installing the engineering model of the D&R Chassis —

P.E. ordered to FAROES to install mod. before 10/31/62

W-234 (CONT)

10/23/62: Cond. inverter of FPN-38 used disarp. — P.E. to HQ to get passport, orders, shots etc for FAROES trip

10/24/62: Reduced size of R35 in D&R Chassis from 33K to 1K & removed diode CR11 — This gave us good zero reset with no distortion of 100KC squarer output, no loading on 100KC to squarer & over a range of adj. of 100KC at R-109 from << 5V.pp (ie till timer stops) until about 8V pp (adj during align for 5V pp) -- will apply this to Faroes equip if run into problems —

DATA: Study of Time Reference Control on HP H06-113BR Clocks vs/ change by absolute reset to the clock comparing the 160,000 usec clock pulse with the ensuing timer divider reset pulses:

Started with dial set for zero error:

TIME REF CONTROL SHIFT (usec)	reset error (usec)
+ 0.5	+ 0.5
+ 1.0	+ 1.0
+ 1.5	+ 4.0
- 0.5	- 0.5
- 1.0	- 1.0
- 1.5	- 1.5
- 2.0	- 1.5
- 2.5	- 2.0
- 3.0	- 3.0

If this phenomena experienced at Faroes, will have to very carefully set Time Reference Controls - this was not experienced when testing the D&R chassis sent to Faroes when tested here — then we got 0 error with changes of time reference control over a range of ±2½ usec with 10 usec errors past this range — will have to check this out!!!

10/25/62: Correcting minor errors found in FPN-38 instruction write up for timing mod. — getting spares need together — writing up something for taking to Faroes on the alarm circuits being prepared —

W-234 (CONT)

10-26 to 11/29: P.E. away installing FPN-38 timing mod. in the Eide Faroe loran station timers. See report & log of trip included in the Project folder —

During this period, assembly of the AN/FPN-41 timing mod. progressed — timing cabinet panels were received & etched & wiring up of No 1 cabinet is underway both unit chassis were installed and satisfactorily tested in the FPN-41 timer — The 100 kc amplifiers were redesigned slightly to make them pre-tuned (non variable) & one copy is satisfactorily operating under test —

11/30 to 12/4: Investigating the FPN-38, 0200 board circuits in the attempt to determine why the Q6-Q7 & Q10-Q11 transistors appear to be sensitive to changes in their characteristics causing improper resetting of the timer? This was discovered at Eide during mod. installation & testing

Also building a FF circuit similiar to the one made at Eide in order to have the correct waveforms for modifying the reset-alarms to the 4 second system. The alarm to indicate that the clocks are tracking is breadboarded & will have to be tested using the new 4 second waveforms (this will be designed to give alarm when clocks are more than 20 usec out of step) — this necessary since divider reset from the two timers are not occuring identically in time.

12/5/62: Looked at 0200 board (FPN-38) at Q6-Q7 Q8-Q9, & Q10-Q11 to determine their state during inhibit with a reset occuring 10 usec before & 10 usec after the zero correct time & found that all F.F. & the F.B. Binary are in the same state during inhibit — thus the 0200 board is turning off properly (as confirmed at Eide) at the beginning of inhibit and the discrepancy in reset is occuring at the end of inhibit and when the divider resumes counting (also as confirmed by scope photos taken at Eide — See project folder)

Q10 Hi (4v)
Q11 Lo (0v)
Q6 Hi (4v)
Q7 Lo (0v)
Q8 Hi (4v)
Q9 Lo (0v)

Changed the Q10-Q11 transistors in one 0200 board using 2N167 with matched Betas ( ) still get 10 usec discrepancy and not consistent — sometimes early & sometimes late — measured β of transistors taken out & they were ___ and ___ respectively

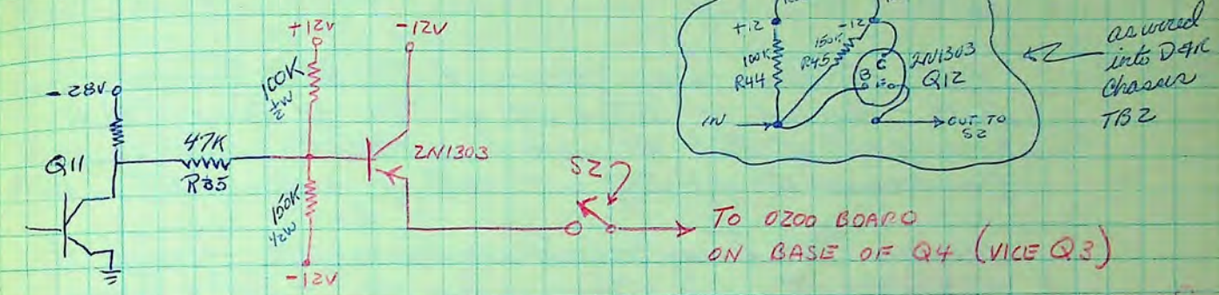
Now changing the Q6 & Q7 using matched transistors with

W-234 (CONT)

Betas of ___. this procedure did not seem to help — neither 0200 board resets properly —

12/6/62: Continuing with investigation of the 0200 board problems and reasons for reset to sync off —

Finally decided to modify inhibit feeding circuit: Refer to schematic in Interim Rpt No 4 —



(this provides a good reset to zero with both 0200 boards)

no further changes to 0200 board plus 12 resistor removed from emitter of Q3-Q4 & circuit returned to normal configuration — change lead from base of Q3 to base Q4 —

Continuing with construction & wiring of the FPN-41 timing cabinet

12/7/62: Changed to two 0200 boards back to original configuration by taking out emitter resistors in 100kc square — both board work OK now using above inhibit coupling circuit —

Cond. up alarms to modify for use with 4 sec reset system —

12/10/62 Cond. with FPN-38 alarms — logic board now working OK & nearing success with alarm board using 4 second information — fabricated permanent mod board for D&R chassis with above circuit in the inhibit path — continuing with wiring up of FPN-41 timing cabinet

12/11/62: Cond. with FPN-38 alarms — wiring of FPN-41 timing cabinet —
12/12/62 writing revised FPN-38 report & test

W-234:

12/12/62 → 12/4/62: Completed rewiring Timer ~~tracking~~ Jump Alarms and some trouble in testing — had to scave to allow workers FPN-38 AFC and blink mod projects — completed test of breadboard of Clock Tracking Alarm & started building unit — no more work on FPN-41 timer mod due timer obligation to W-247 —

1/7/62: Returned to jump alarms for test — cont with write up on alarms & mod to timing mod FPN-38 — checked out FPN-41 timing cabinet for eventual test of system when can get timer —

1/8 → 1/18: Built the Timer Jump Alarms & the Clock Tracking Alarm built — checked & tested OK in FPN-38 Timing Mod — Rough draft of FPN-38 report & installation inst compl & working on the operating inst write up following return Pat #.

Wiring of FPN41 Timing Cabinet almost complete — need to straighten out wiring & check for being OK — test of Timing Chassis #1 OK — need to check out entire system when can get at timer — 100kc amp (latest mod) seems OK — building two final 100kc amps —

1/21 → 2/1/63: Completed all wiring in FPN-41 Timing Cabinet No1 & working on wiring Timing Cabinet No2 — Still have not be able to get on FPN-41 timer to test mod. — 100kc to timer now coming thru Q shifter & amp in Timing Cabinet No1 & is about 10v pp at the timer — seems to operate OK — all parts of Timing Cabinet No1 seem to work OK —

All final tests completed on FPN-38 alarms & timing modification improvements and all material has been assembled for shipping to Eyde Loran Station — Interim Report No2 covering the FPN-38 alarms — instr for install & oper — has been written and is being reviewed — data taken on this new system for other basic rates:

SO: each reset w/ 4sec trig — way ½ Per OK — Reset OK w/ 4sec system
LO: " " " " — " " " — Reset OK " " "
HO: skips two resets " " — way 3rd " " — Reset NG " " "
SSO: same as SO _____ OK _____
SLO: same as LO _____ OK _____
SHO: same as HO _____ NG _____

∴ The 4 second reset system will be OK for all S&L basic rates but limited use on H rates:

W-234:

2/11/63: Re-Connected the FPN-41 timing modification into the FPN-41 timer and tested satisfactorily. — all appears to be operating OK — reset is up in 0.1 sec — 1PPS trigger and LSTS appear to be inserted properly — will have to measure exact 1PPS trigger location w/ respect to the first M pulse of the group — letting equipment run while working on final report — shipping instr for timing mod have been received —

3/15/63: Position of 1PPS (when trigger is of proper amplitude to make correct 100kc gate in XMTR driver —) is exactly 2000 usec ahead of first Master trigger — all OK — testing still

3/28/63: Con't to test timing mod in 41 — all still OK. — put 42 on air w/ 1PPS — all OK — pulse stable — proper ϕ code — 500 usec of 100kc after trigger is more than enough 100kc —

3/29/63 Took timing mod out of timer — getting it together for shipping to LTS Caralina Beach — Writing final report